Final Report for ECG 620 (OpAmp Project)
May 8th, 2019
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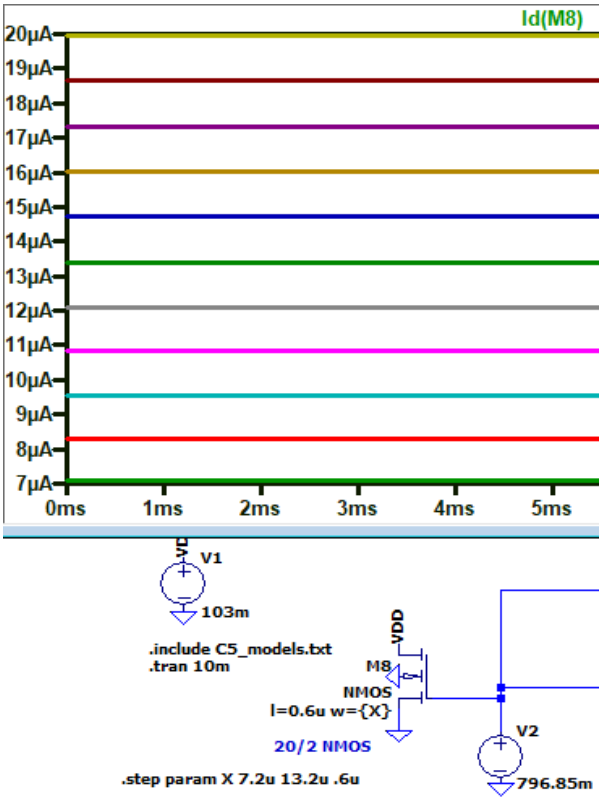
Introduction

The project specifications were not completely satisfied with PSRR and CMRR being the biggest culprits. However, the Gain-Bandwidth product is excellent. The use of a more sophisticated topology, such as those utilizing OTAs, would assuredly improve the situation. In addition, I believe power draw is rather large. The final OpAmp schematic is in **OpAmpBeta2.asc**.

Design Process

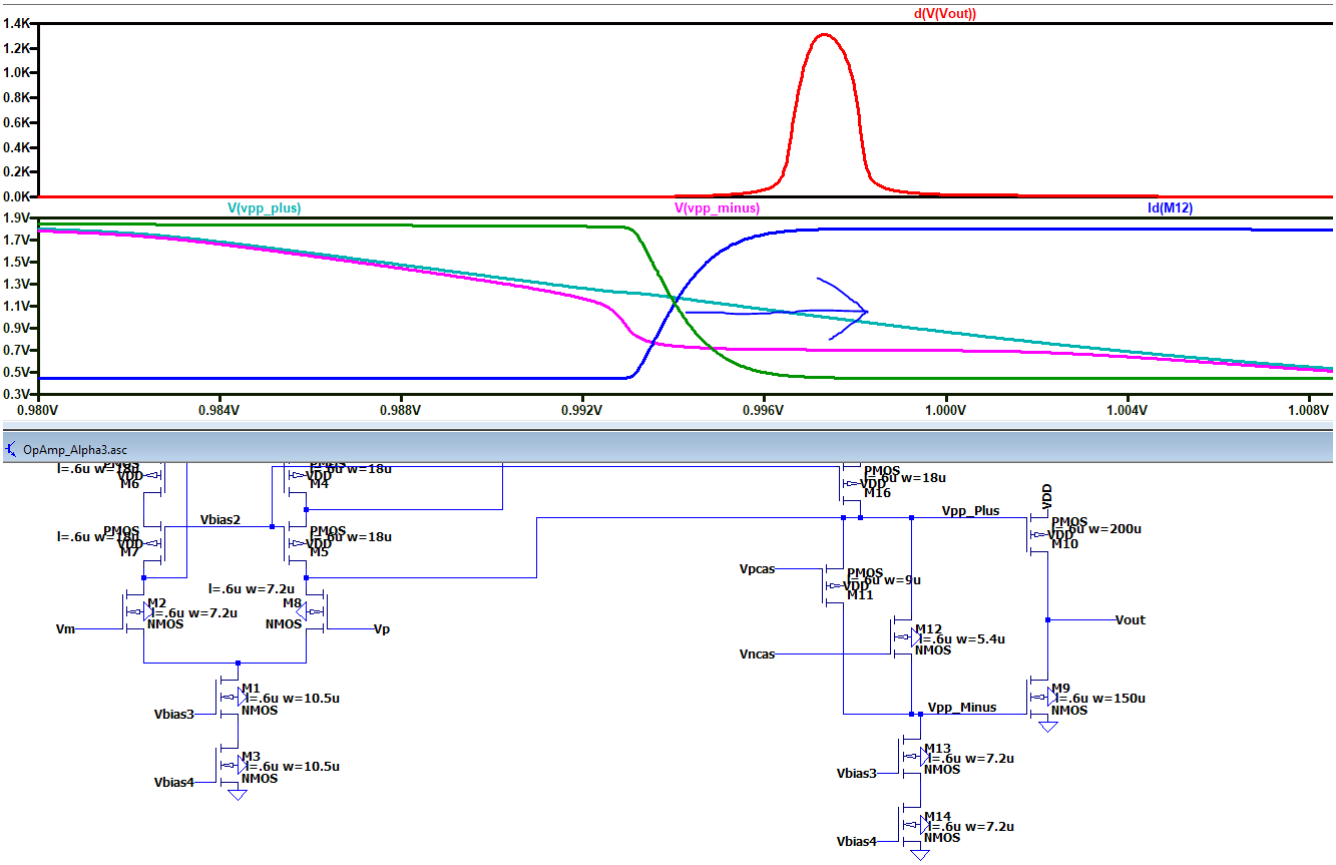
The first step in the project design was to select appropriate sizes for the biasing circuit. This requires that threshold voltages be determined. From the C5_models.txt file values of VTHN = 0.67V and VTHP = 0.92V were chosen. (Later, more precise values of Vthn=0.64V, Vthp=0.86V were determined by simulating and determining gate-source voltage when 1uA of drain current flows.) An overdrive voltage of 60mV and a target current of 8µA were used to select standard widths of NMOS and PMOS transistors. (Length was always standard 2*scale = 0.6µm.) The testing circuit can be seen in BetaTestNMOS2.asc and BetaTestPMOS2.asc. **Figure 1** is an example simulation from previous:



I believe Alpha1 and Alpha2 OpAmp circuits are from this stage of the design, where it became clear that more gain was required. The bias circuit was redesigned with first 5µA, then finally about 2µA of current per branch and ostensibly about 50mV of overdrive voltage. This led to sizes of .6µ/12µ for NMOS and .6µ/30µ for PMOS. Designing the BMR is tricky when close to the subthreshold region as current does not scale linearly with width, as our equations would expect. Design is mostly choose k=4 (final design, k=3) and plug in a good resistor value by experimentation.

A few other notes about the reference relate to how I tried to obtain more gain. Note in Fig 2 below how the floating current mirror is not active exactly where the region of maximum gain exists.

Figure 2

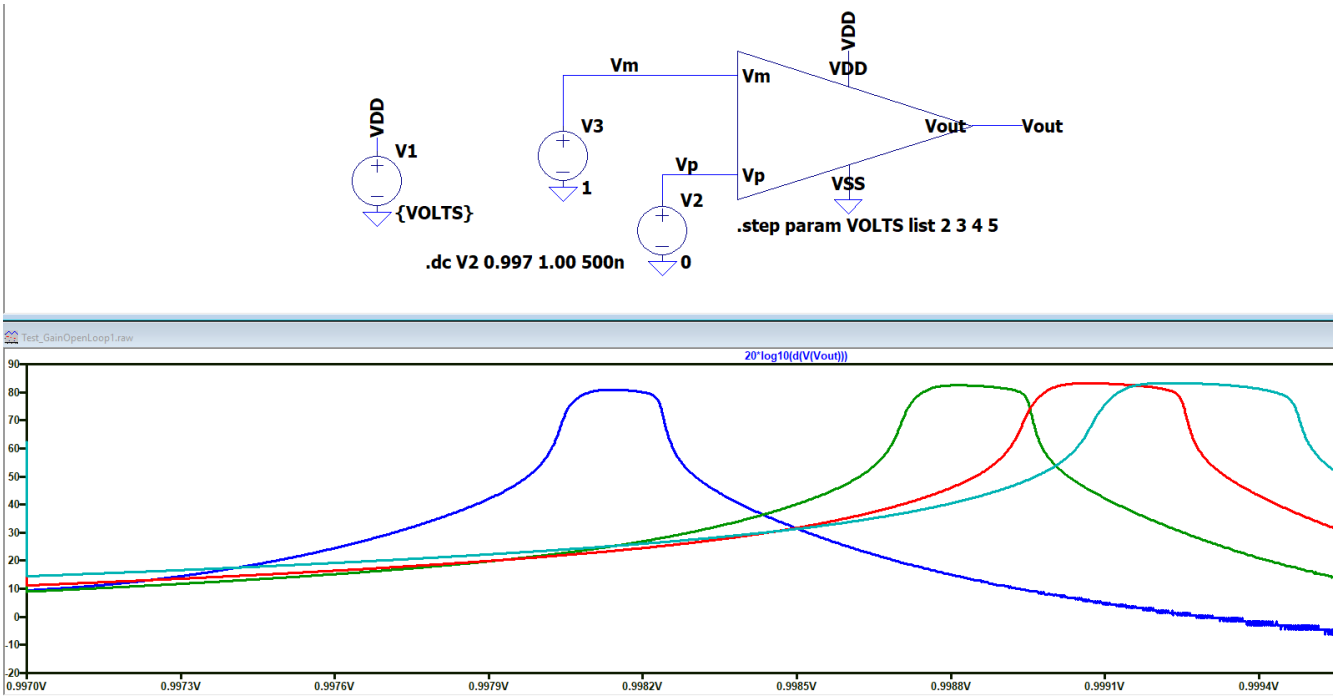


One method employed to improve gain is to move the Vpp_Minus node lower. This is achieved by lowering the Vncas voltage. Note in the C5Reference.asc circuit that M30, used to generate Vncas, is extremely wide. Vbias2 was also tweaked in this manner to be a bit lower.

Specifications

The original specification calls for 80dB of gain at voltages between 2 and 5 volts. This specification is met in figure 3.

Figure 3

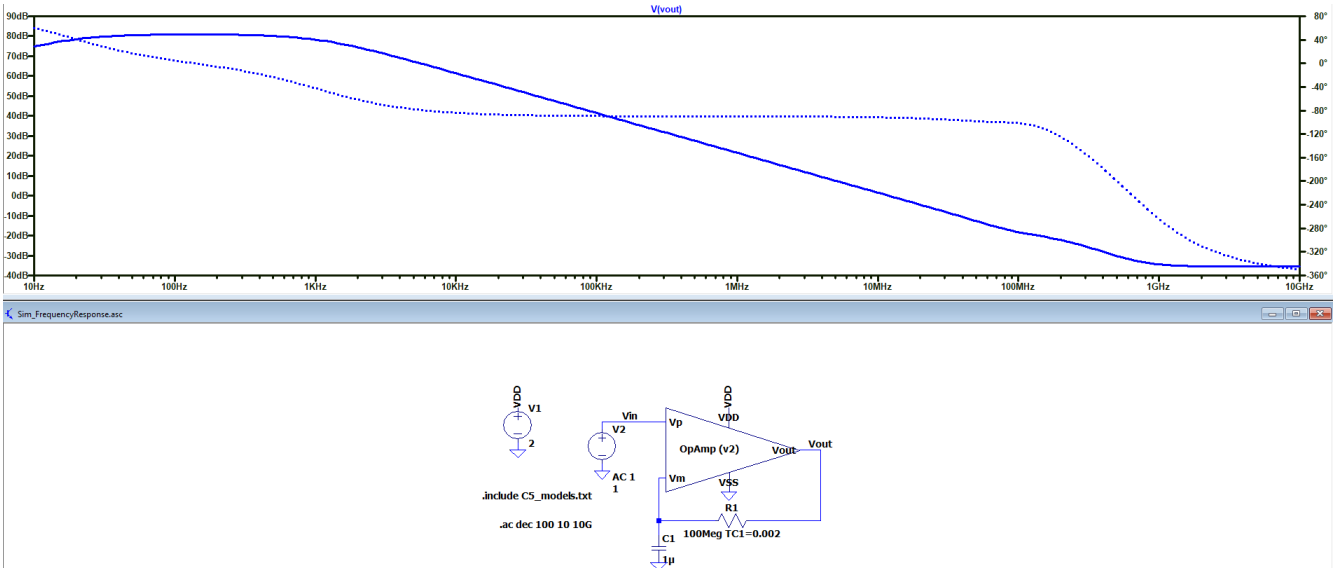


The most difficult part of the compensation design (aside from understanding it) was getting capacitance values. Looking in the C5_models.txt file we see that tox = 1.39x10^-8m. Cox' = [epsilon]*3.9/tox, where 3.9 is relative permittivity of SiO2: (8.85x10^-12)*3.9/1.39x10^-8 = 2.48fF/µm^2. Cgs' = 2/3*2.48fF/µm^2*0.6µm = 0.99fF/µm. Cgd involves CGDO parameters, and finally: Cgd' =0.2fF/µm (of width, NMOS) and Cgd' = 0.29fF/µm (PMOS). We perform simulations to determine transconductance and resistance parameters of gm1, gm2, R1, R2: C1 = 161fF = Cgd(M5) + Cgd(M8, with miller effect gain of 59). C2 = small + load. Cc = at least 174fF. R1 = 1.3M, R2 = 932 (but I actually decreased size of output buffer after this, so these values are not completely correct), gm1 = 48µA/V, gm2=~10mA/V (estimated with **Sim_gm1.asc**, **Sim_ro2.asc**, and related circuits).

Results: fz = 9GHz, f1 = 75kHz, f2 = 2GHz. A random 1pF capacitor was added as compensation and did not seem to cause much harm.

In Fig. 4 we can see the frequency response meets the requirement of 1MHz Gain-Bandwidth Product as the unity-gain frequency is about 11MHz.

Figure 4



Other parameters

Power Supply Rejection Ratio unfortunately did not meet specifications. The next figure shows PSRR- is not working very well.

Figure 5

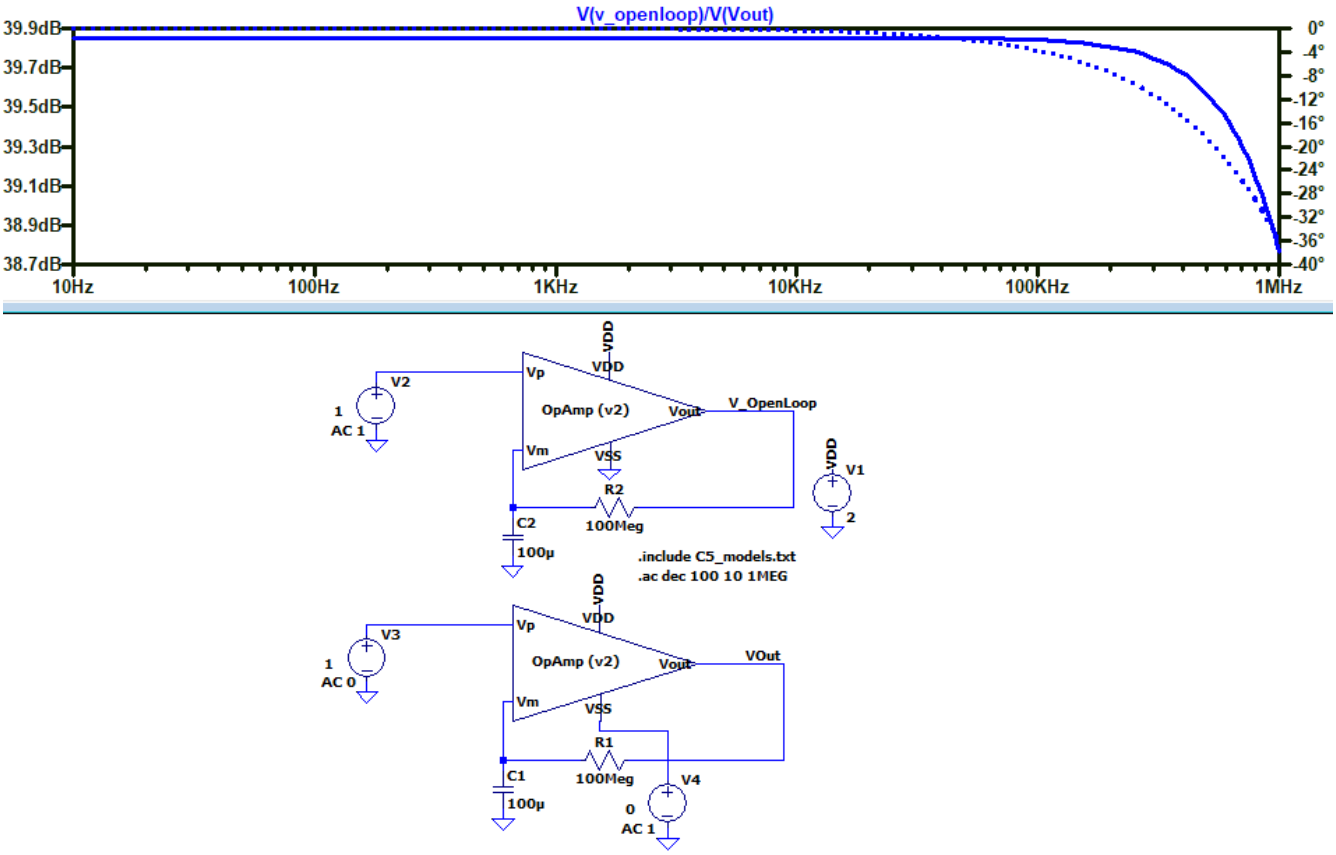
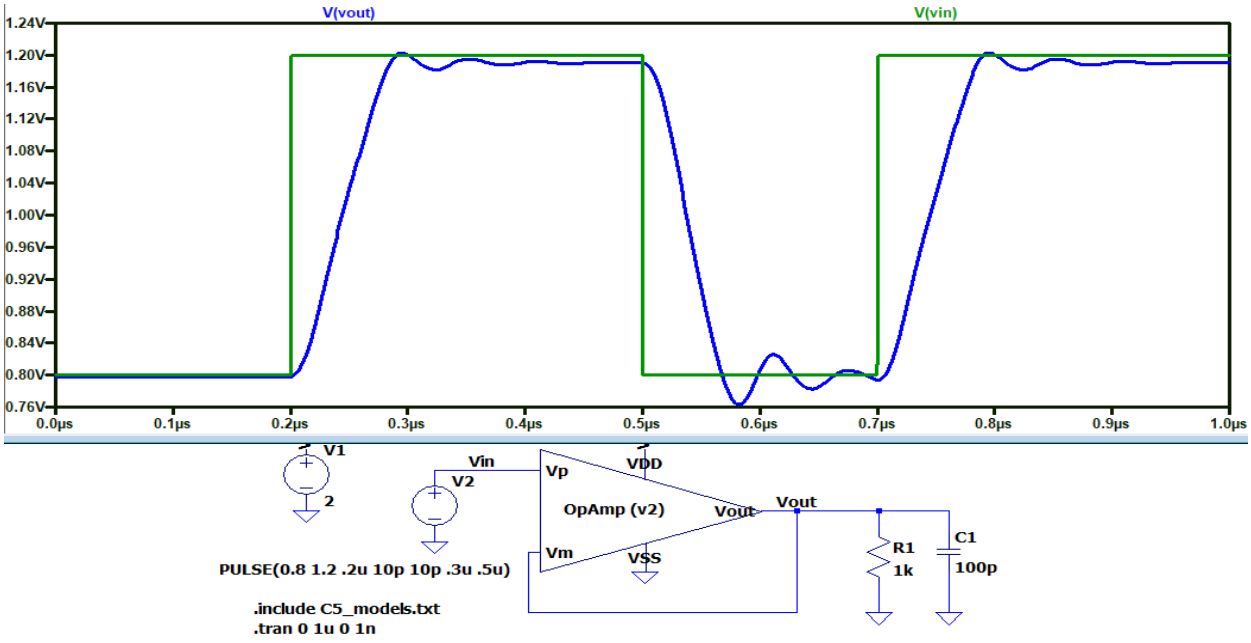
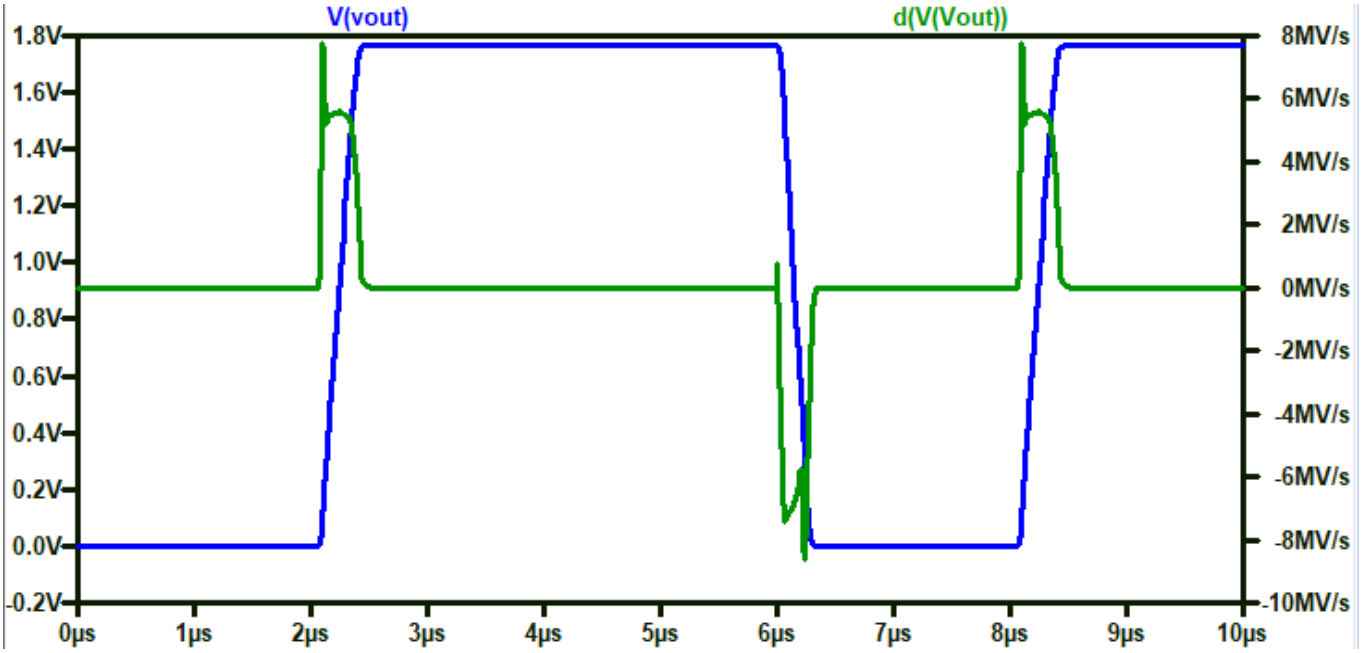


Figure 6



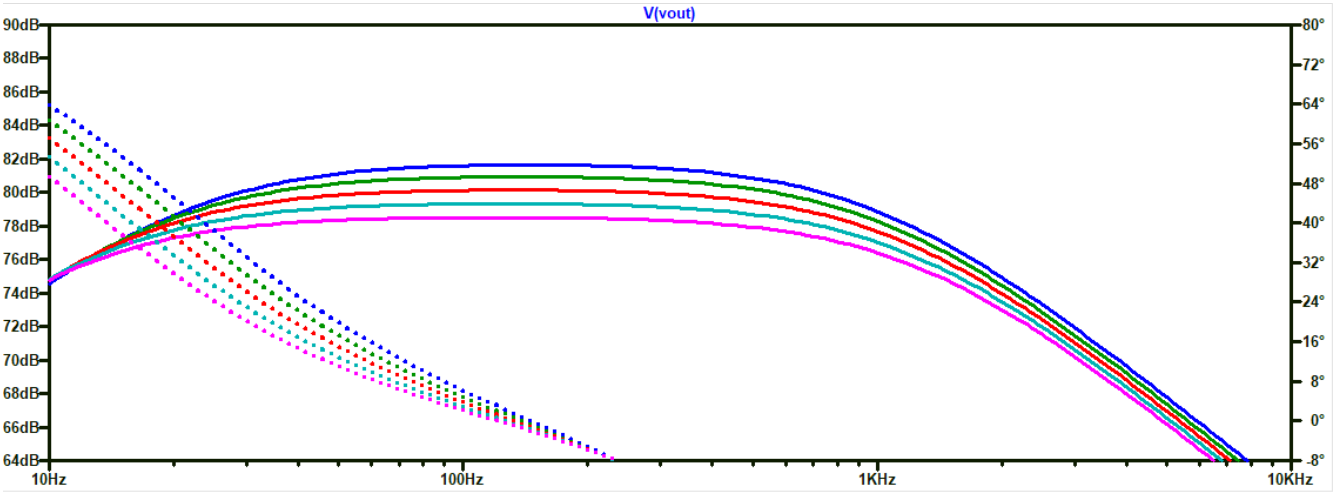
Step response shows some ringing but seems to be fine. See Sim_StepResponse.asc. Slew rate is usually above 5V/µs (Fig. 7) so we may have an over-engineered AB-type output buffer.

Figure 7



Another potential misstep is the failure of a few temperatures in a param list from 0 to 100 degrees to reach open-loop gain of 80dB as seen below.

Figure 8



Power

The power simulation (Sim_PowerConsumption.asc) shows current draw of about 1mA, but I recall that some of the AC simulations showed up to 75mA. It's not great, but better than it was before.

Conclusion

I would have liked to try the OTA topology to see what it could do, but was essentially locked into this design by shortage of time.

Table

VDD	Unity-gain Frequency	Slew Rate
2V	12MHz	5.1V/µs
3V	12MHz	6V/µs
4V	13.6MHz	6.2V/µs
5V	12.1MHz	~7V/µs

Note that negative slew rate (output toward ground is slightly faster).