# Design and Analysis of a multi-rail DC-DC Power Supply

By Jason Silic – March 22, 2021

This report will describe the design and simulation of a switching DC-DC power supply based on the project for Dr. R. Jacob Baker's ECE572 power supply class. The course information for this specific project can be found at http://cmosedu.com/jbaker/courses/ece5472/f10/ece5472.htm. The project involves replacing the on-die power supply circuitry of a DRAM chip with a custom chip using the economical 0.5µm C5 process. Some external components may be used, including a diode, a large inductor, and capacitor for the output filter.

Two standard buck converters are used to convert the input voltage, ranging from 3V to 5V, to the primary output rails at 1.25V and 2V. These two rails can supply up to 100mA of current. A charge pump architecture is used to produce an additional output voltage at -500mV and 100µA max. Voltage regulation is achieved with a "Type II" error amplifier controlling the PWM (Pulse Width Modulation) for a large MOSFET supplying energy to the output.

## General Theory of Operation

We begin our study by deriving the transfer function of our control loop. We can then examine the stability of the loop in idealized simulations (both AC and transient) before using real components and verifying our design with a full (and slow!) transistor-level simulation. In Figure 1 below we can see the Type II error amplifier is used to set the duty cycle of the main switch of the power supply. This signal is then fed to the output filter and feedback from the output voltage completes the control loop.

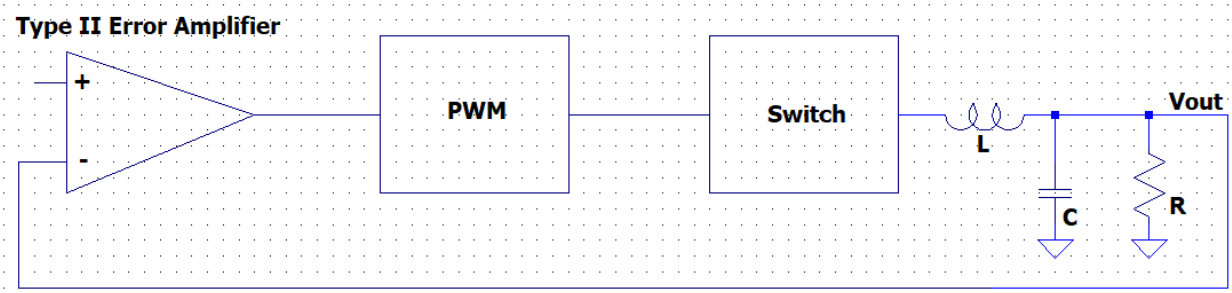


*Figure 1 – Control Loop*

Let's determine the forward gain and exclude the feedback for now. The Type II error amplifier is shown in detail with associated R and C components in Figure 2. We can determine the gain of this block by remembering that the current flowing through the input impedance (excluding the common-mode voltage, Vref) is Vin/R1 and is equal to the current flowing through the op-amp feedback impedance.

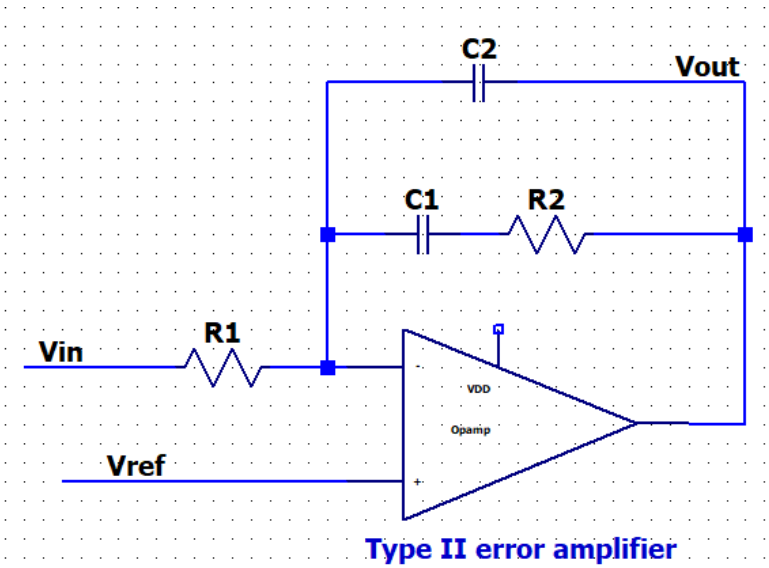


*Figure 2 – Type II error amplifier*

In equation form, with s = jω:

$$\frac{V_{in}}{R_1} = \frac{-V_{out}}{\frac{(R_2 + \frac{1}{sC_1})\frac{1}{sC_2}}{R_2 + \frac{1}{sC_1} + \frac{1}{sC_2}}}$$

Rearranging to solve for Vout/Vin and multiplying top and bottom by $s^2C_1C_2$:

$$\frac{V_{out}}{V_{in}} = \frac{-\frac{1}{R_1}(sC_1R_2 + 1)}{s^2C_1C_2R_2 + s(C_1 + C_2)}$$

Multiplying top and bottom by $R_2$ and factoring $sC_1R_2$ from the denominator results in:

$$\frac{V_{out}}{V_{in}} = \frac{-\frac{R_2}{R_1}(sC_1R_2 + 1)}{sC_1R_2\left(1 + \frac{C_2}{C_1} + sC_2R_2\right)}$$

We can simplify the analysis here by assuming that C2 is much smaller than C1. We can then see that we have a gain term of $R_2/R_1$, a zero at $1/C_1R_2$, a pole at zero, and a pole at approximately $1/C_2R_2$.

The output of the error amplifier is sent to a comparator where it is compared to a ramp waveform. As seen in Figure 3 the output of the comparator is high when the comparator output (vc) is larger than the ramp voltage. If the ramp voltage ranges from 0 to $V_p$ then we can write that the output duty cycle, D, is:

$$D = \frac{V_c}{V_p}$$

Where $V_c$ is the output of the amplifier. The gain of the PWM block is thus $1/V_p$. The switch at 100% duty cycle simply passes the source voltage, $V_s$. We can thus deduce the gain of the switch:

$$V_{sw} = DV_s \text{ or } \frac{V_{sw}}{D} = V_s$$

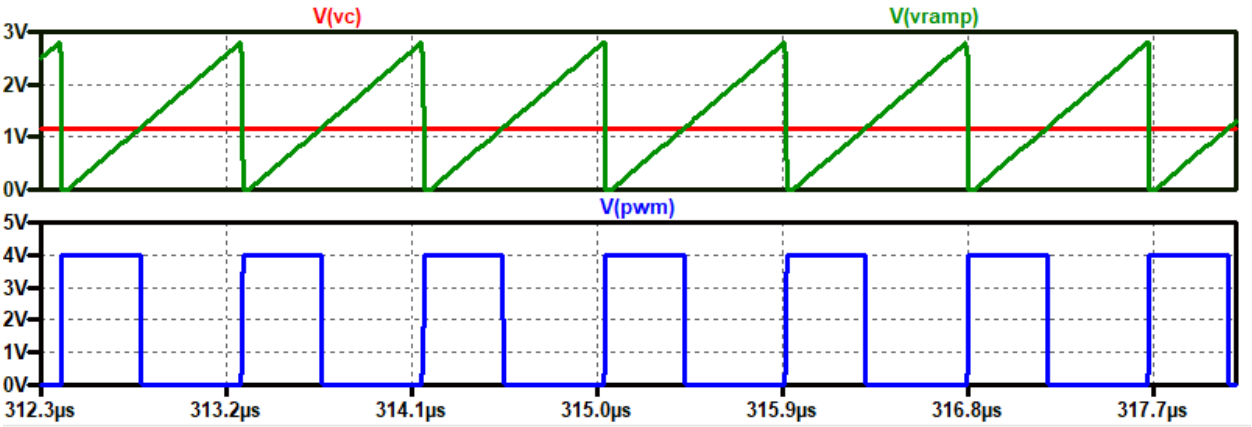


*Figure 3 – Generating the PWM output*

Thus, the gain of the switch is $V_s$. The final block we have to determine a transfer function for is the output filter. Referring to Figure 1 note that the parallel combination of the *C* and *R* results in an impedance of:

$$\frac{R/sC}{R + 1/sC} = \frac{R}{1 + sRC}$$

The resulting transfer function is then:

$$\frac{\frac{R}{1+sRC}}{sL + \frac{R}{1+sRC}} = \frac{R}{R + sL + s^2RLC} = \frac{1/LC}{s^2 + \frac{s}{RC} + 1/LC}$$

The complete transfer function of the forward path is thus:

$$H(s) = \left(\frac{1/LC}{s^2 + \frac{s}{RC} + 1/LC}\right)\frac{V_s}{V_p}\frac{-\frac{R_2}{R_1}(sC_1R_2 + 1)}{sC_1R_2\left(1 + \frac{C_2}{C_1} + sC_2R_2\right)}$$

Using the quadratic equation, the output filter has poles at:

$$s = \frac{\frac{-1}{RC} \pm \sqrt{\frac{1}{(RC)^2} - \frac{4}{LC}}}{2}$$

Note that as R becomes larger (load is small) the poles move close to the imaginary axis. This results in more “peaking” of the transfer function near those frequencies and less stability. Our power supply will require a minimum load to avoid becoming unstable. The error amplifier also has the poles and zero as discussed above.

We now need to review classic control theory to determine criteria for stability. Consider the simple system in Figure 4. The output is the signal at the summing node multiplied by A, the forward gain.

$$Out = (In - B \cdot Out)A$$

Solving for Out/In:

$$Out(1 + AB) = In \cdot A$$

$$\frac{Out}{In} = \frac{A}{1 + AB} = \frac{1}{\frac{1}{A} + B}$$

In our control loop the feedback factor is generally unity. If B is 1 then the above equations go to infinity (system is unstable) when A = -1. In our design this is when the forward gain is 0dB and the phase shift is 180°.

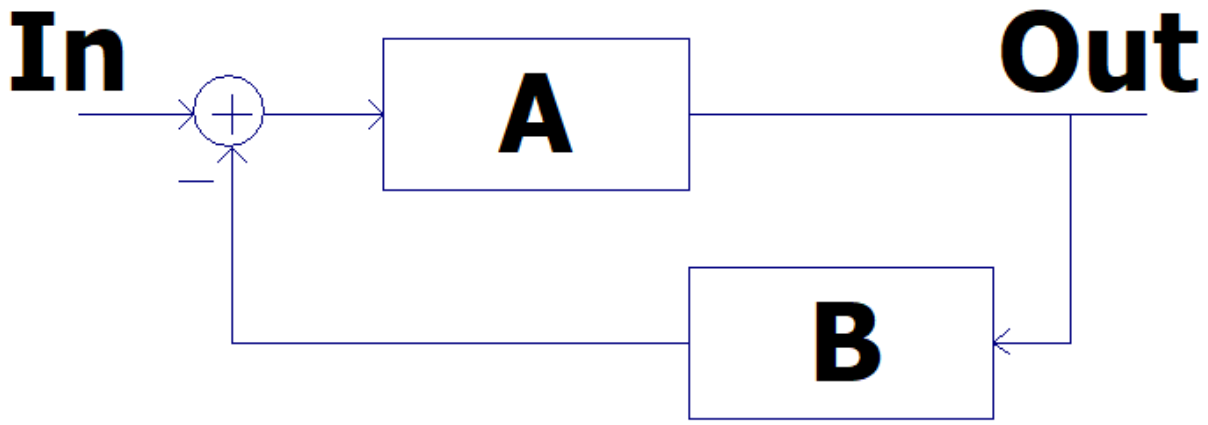


*Figure 4 – Abstract System Representation*

## Design of the Control Loop

The first thing we should try to understand is the frequency response of the error amplifier. The pole at zero results in a constant decrease in gain of 20dB/decade. In the circuit **ZeroPlotter.asc** the second pole can be ignored because C2 is so small. We therefore expect the frequency response to decrease at 20dB/decade and then flatten out at the zero. The phase response will begin at -90° from the pole and then increase to 0° in the two decade range centered on the zero frequency (this is basic Bode plot theory). In this simulation we have a 10k resistor and values for C1 of 15.9nF, 159nF, and 1.59µF for zeros at 1kHz, 100Hz, and 10Hz, respectively. This can be seen in Figures 4 and 5. Note that at higher frequencies C1 is close to a short and the gain of the opamp is effectively 1, or 0dB. This is actually the ratio R2/R1 as discussed earlier.

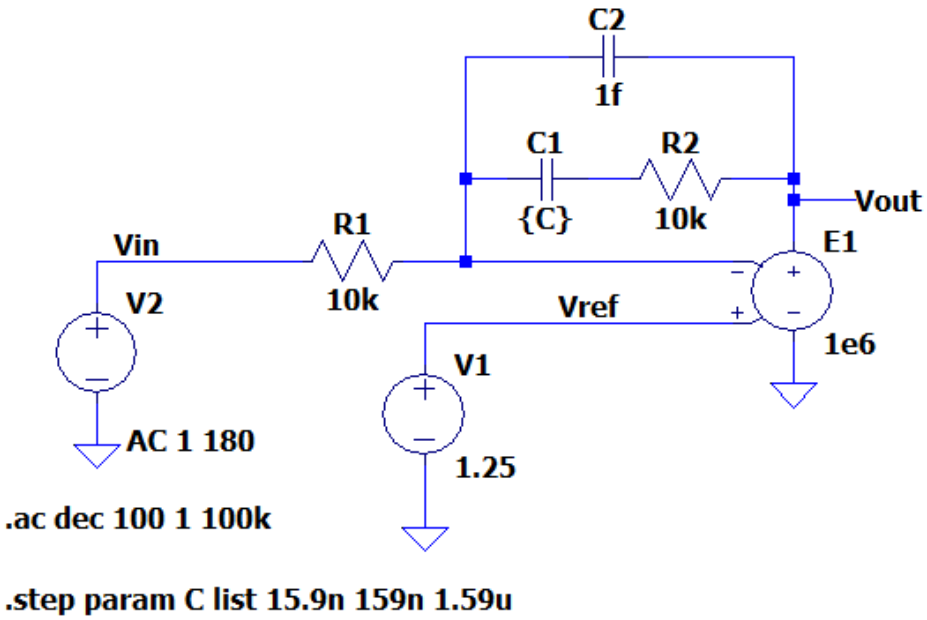


*Figure 5 – Schematic to plot frequency response of Type II amp*

When C2 is larger its pole moves down to frequencies closer to our range of interest and contributes to additional roll-off at higher frequencies. We want less gain at higher frequencies to improve stability (for example, step functions and impulses have high-frequency content we prefer to damp). In Figure 7 we have a capacitor of 159pF, which results in a pole of 100kHz with R2. The unfortunate effect of this pole is an increase in the phase shift back toward -90°.

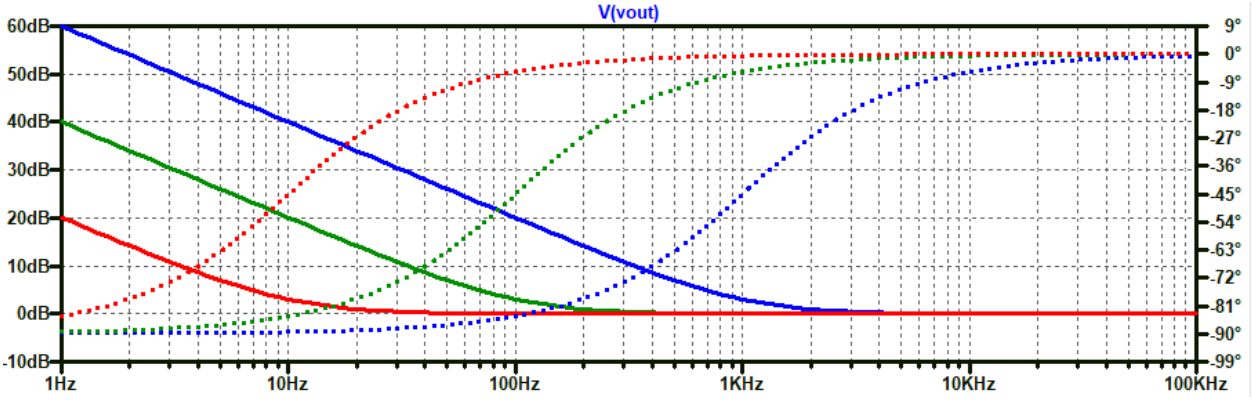


*Figure 6 – Frequency response with zeros at 10, 100, and 1kHz*

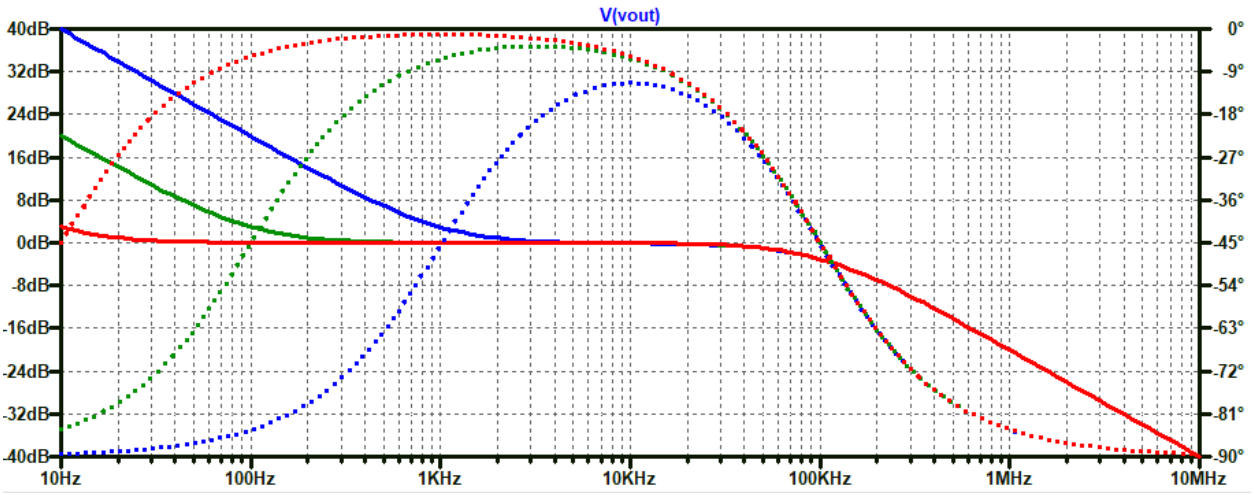


*Figure 7 – Frequency response with additional pole at 100kHz*

The next step is to consider the output filter. The poles from this RLC network can be determined from the above equation for the output filter. Note that the $(RC)^2$ term is much larger than the LC term and essentially disappears because it is in the denominator.

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

We now turn to the open loop frequency response of the system and see that these poles produce "peaking" around $f_0$. In **IdealStability1.asc** we examine the stability of the forward loop as we design the control circuit for the 1.25V supply. Initially it was considered expedient to avoid discontinuous current in the inductor, which necessitates having a large L and small C. Assuming a 1MHz ramp signal we see that at 10% duty cycle the switch can be off for 900ns. Assuming an ideal diode and approximating with constant voltage across the inductor:

$$\Delta I = \frac{V}{L}\Delta T$$

With 1mA flowing on average our peak will be 2mA; a voltage of 1.25V is developed across the inductor with an ideal diode. We see that our minimum inductance in this situation is 694µH. The inductor can be smaller if the minimum load current is larger. Note that we eventually find that maintaining continuous current is not required and we can use a much smaller inductor.

For our initial design we selected a resonant frequency for the output filter of about 2.5kHz. In general a higher frequency here will result in smaller, cheaper components while a lower frequency will smooth the output voltage and current more effectively. We will return to this point as we improve the design.

In [1], pg. 1206, we have a general guideline that $f_z$, the frequency of the zero, should be less than or equal to $f_0$. In Figure 9 we note the zero is at 1/(2π*5k*15.9n) = ~2kHz. It is helpful to have the zero at a higher frequency so that we improve the gain at lower frequencies. Recall that gain increases by 20dB/decade as frequency decreases from the zero.

Note in the AC simulation seen in Figure 9 there is significant peaking at the output filters resonant frequency, $f_0$, of 2.5kHz. This peaking rises above 0dB, indicating we may have stability issues. Note that

as the load resistance increases (smaller load) this peaking becomes more pronounced. We will return to this topic soon and develop a method of ensuring a minimum load current.

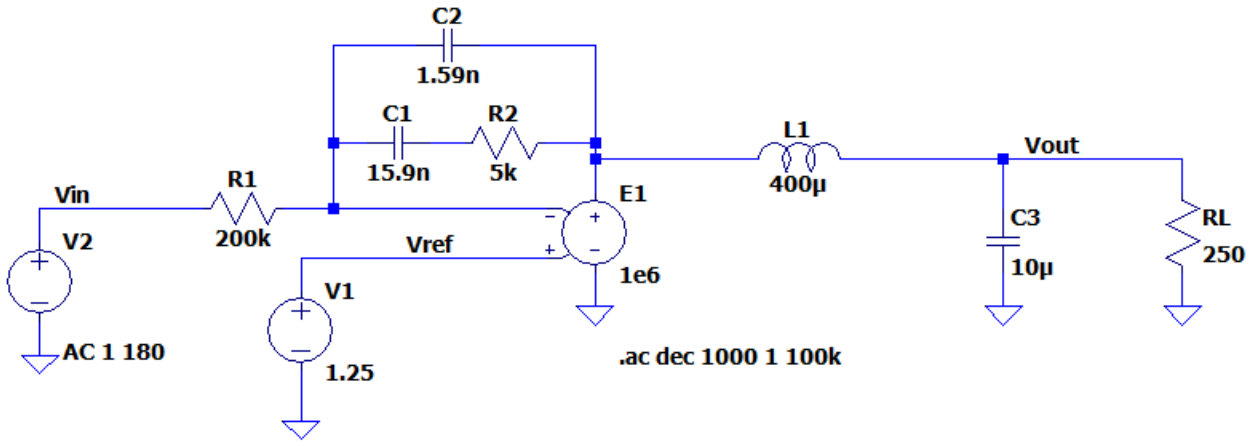


*Figure 8 – IdealStability1 schematic*

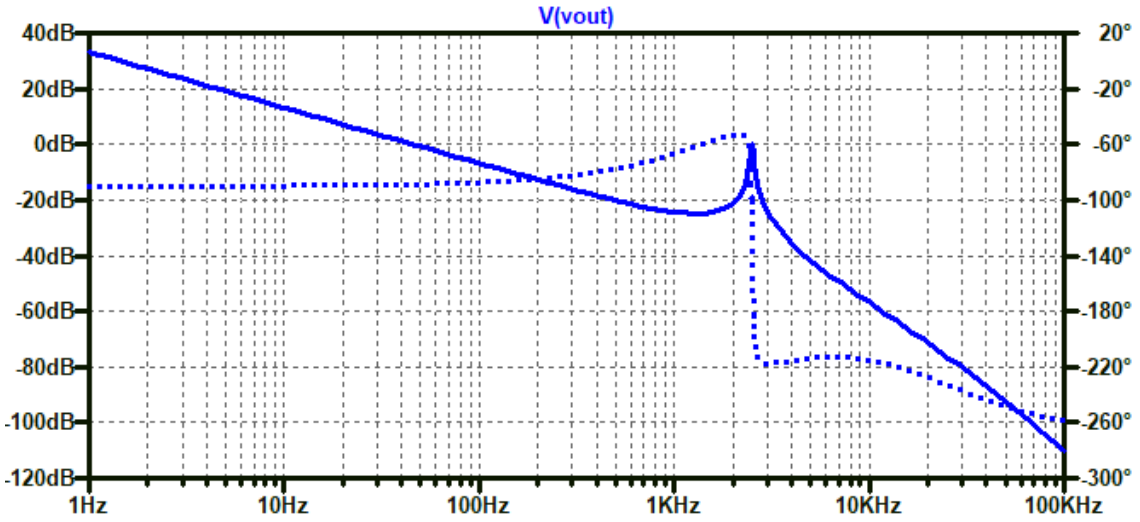


*Figure 9 – IdealStability1 AC simulation*

## Implementing the 1.25V Supply

Let's implement our control loop into an ideal supply and run some transient simulations to determine where we stand. **Supply_125V_1_Ideal.asc** uses the same component values from our control loop and combines them with an ideal comparator and switch. In Figure 10 we can see the output current load begins at 100mA and decreases to 5mA at 5ms into the simulation. Although we do see the output stay around 1.25V there is significant transient overshoot and a ripple at about 2.7kHz when the load is small.

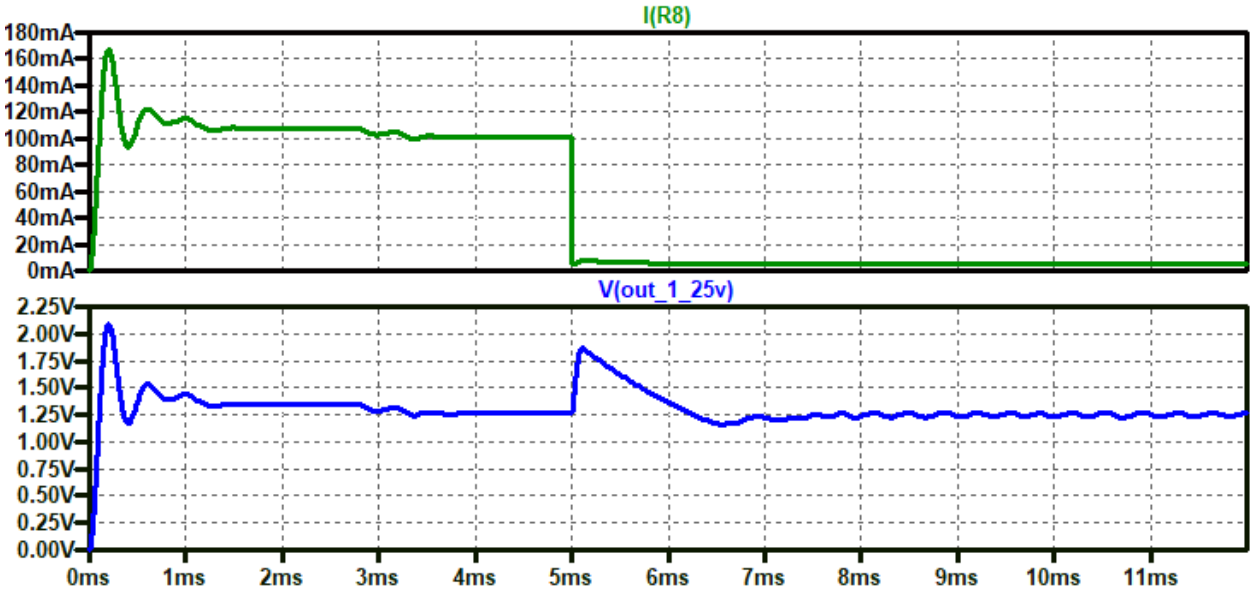


*Figure 10 – Ideal transient simulation for 1.25V supply*

There are a few things we can do to improve the situation. A larger capacitor on the output filter will smooth out some of the transients. Increasing the value of the input resistor will reduce the feedback and gain of the control loop. Another possibility is moving the output poles to a higher frequency which may allow additional gain at lower frequencies where we need it. The effect of this with a larger capacitor leads to a smaller inductor in the output filter. Consider the results from **Supply_125V_2_Ideal.asc** in Figure 11. As the capacitor size increases the size of the voltage transients decrease. Note in this simulation the inductor size is also decreased to 20µH. Note that with a capacitor size of 100µF the output resonant frequency is still 3.5 kHz.

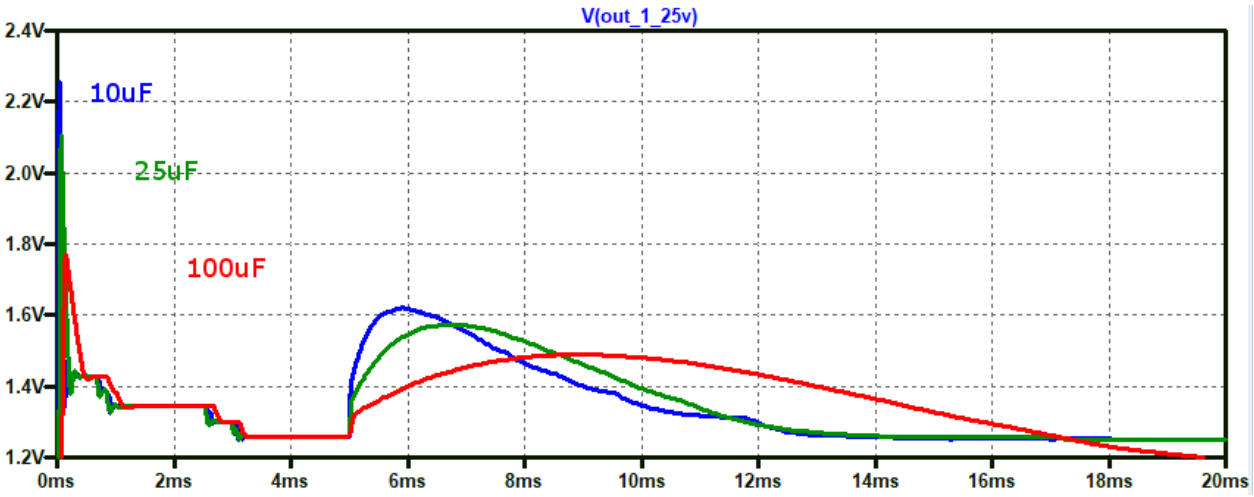


*Figure 11 – Effect of adjusting the output filter capacitor*

We can see greatly reduced transients (with a 100µF capacitor the output voltage never gets above 2V) but also greater settling time with larger output capacitance. There are also some artifacts between 2 and 4ms which are likely due to the ideal components we use.

## Adding minimum load protection

Before we move to real components let's consider how to maintain output stability when there is no external load. One possibility is a resistor in parallel with the load, but this will reduce efficiency when the actual load is drawing enough current. Ideally we will only draw current when the load is not sufficient. Consider that the primary symptom of a small load is the output voltage is too high. We can test this voltage and turn on a NMOS to draw additional current when the output voltage is above a certain level.

To implement this we design a simple amplifier as seen in Figure 12 (**ComparatorSimple.asc**). An important fact to keep in mind is that we do not want this load to be drawing current exactly at 1.25V, which is the normal output voltage. However, we are comparing the output voltage to the 1.25V bandgap reference. To fix this we need to change the switching point of the differential amplifier. The output voltage is connected to the inverting input. Note that M58 has a smaller width than M57 (9µm vs 10µm). This makes the transistor "weaker" so that input Vinm has to push more current through the right branch and drive the output high.

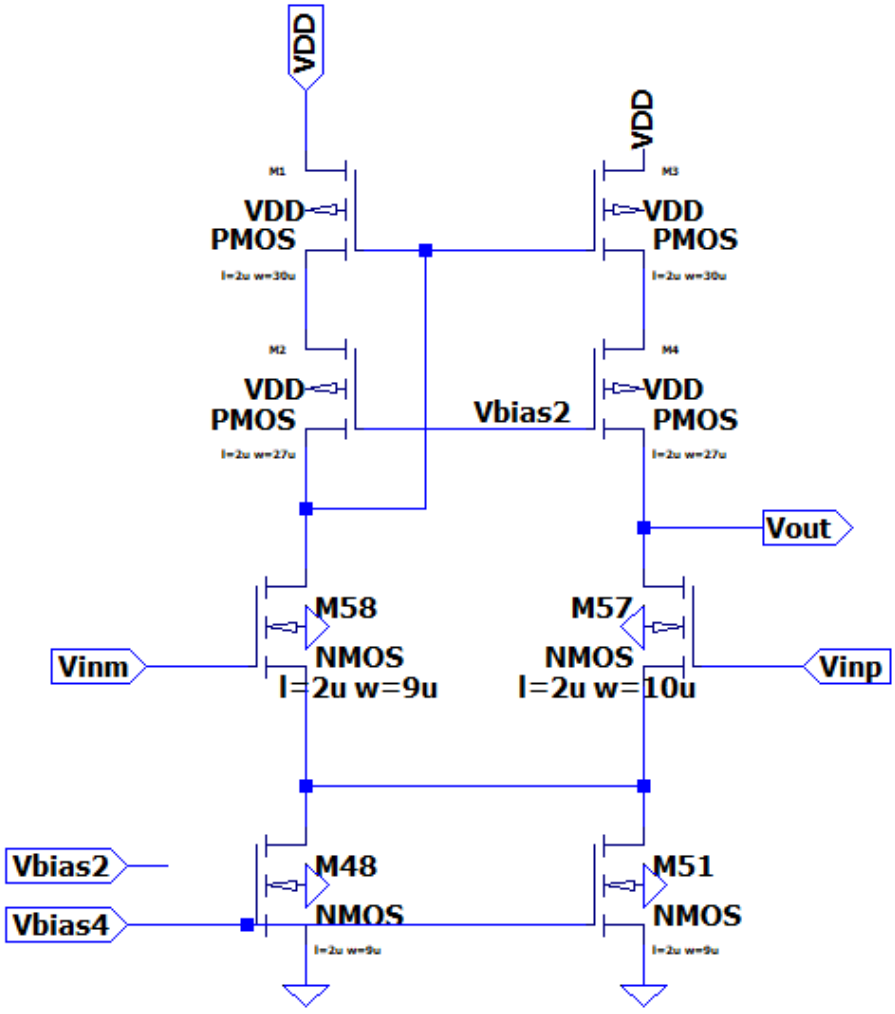


*Figure 12 – Schematic of a diff amp with an offset*

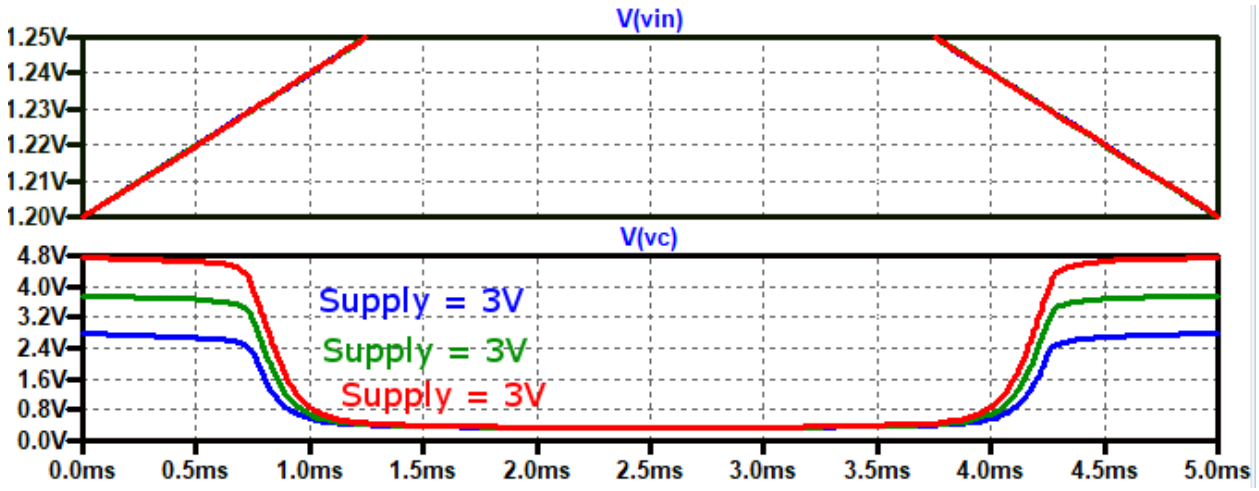


*Figure 13 – Simulation of simple comparator switching point*

In Figures 14 and 15 we see a test schematic (**Comparator_sim2.asc)** and results showing that the switching point is about 10mV above the reference voltage, at 1.26V. (Input Vinm is weaker than Vinp) The 2µm/10µm transistor with m=3 draws about 2mA when activated. This should be sufficient to maintain stability.

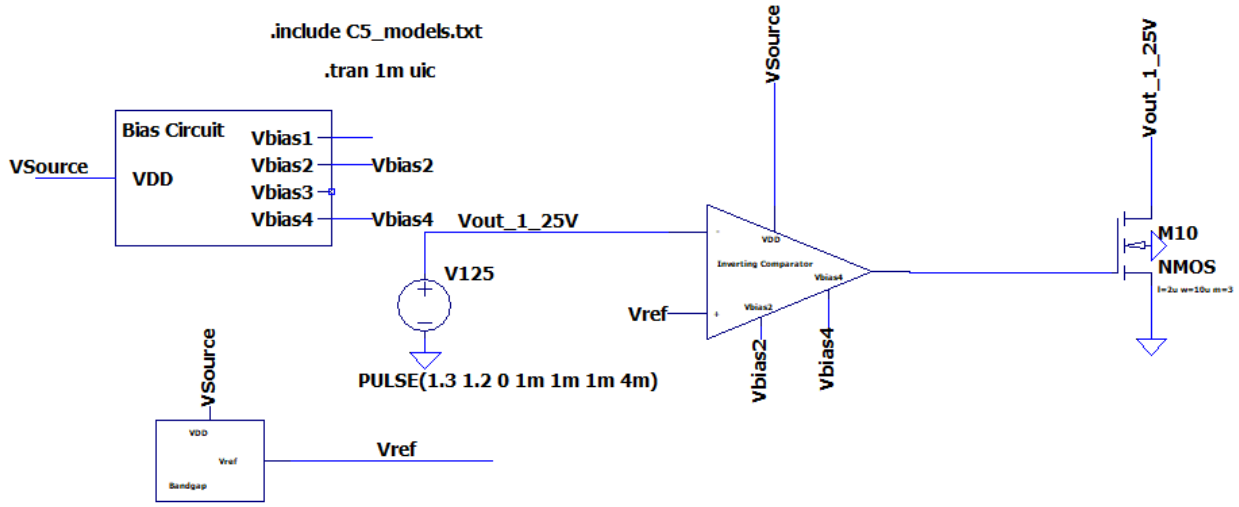


*Figure 14 – Schematic to test the minimum load circuit*

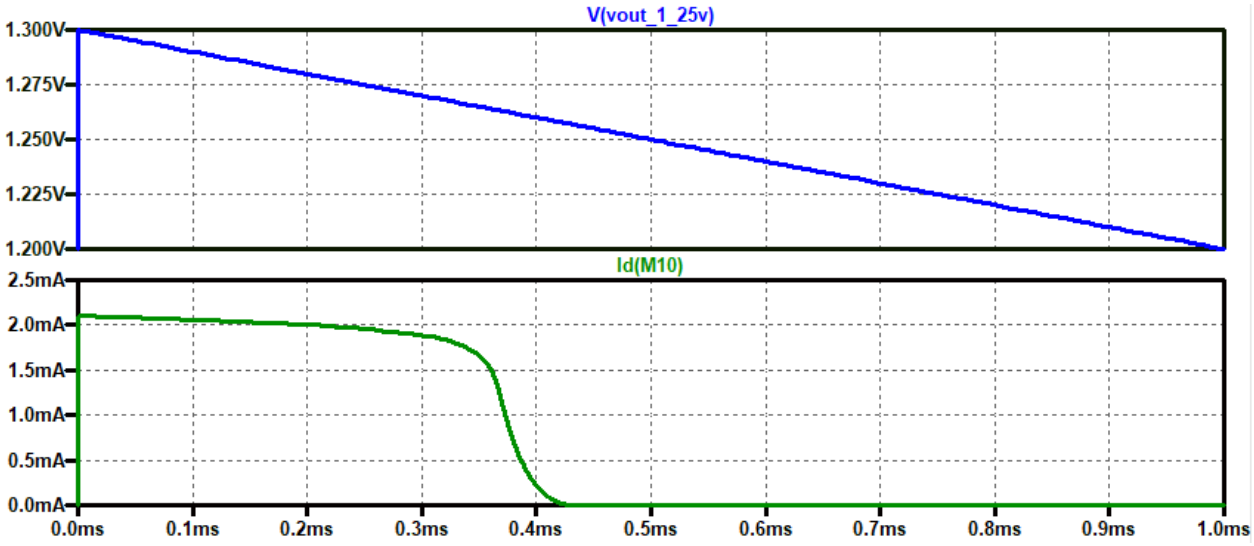


*Figure 15 – Simulation of minimum load circuit*

## Selecting the main switch transistor type

We now pull all the pieces together to design the 1.25V supply. We replace the opamp, bandgap, ramp generator and comparator with the designs using transistor models. The switch is a bit tricky as it needs to be large enough to supply the needed current to the load with a small enough voltage drop. **Transistor_Test.asc** shows how we test our switches. Initial testing showed that the comparator did not have enough "strength" to drive the input capacitance of the switching transistors, so buffers (inverters) are used to make the PWM signal more decisive and square the edges.

Another choice we have is whether to use NMOS or PMOS transistors for the main switch. One serious issue with the NMOS switch is insufficient gate-source voltage in the worst case. If the source voltage is only 3V (the lower end of the acceptable range) and we are trying to drive the 2V output supply then we may have 1V or less for the NMOS switch's $V_{gs}$. Consider the results of the aforementioned circuit in Figure 16. We see that despite being ten times smaller, the PMOS transistor is superior due to its larger $V_{sg}$. Even for the 1.25V circuit the PMOS conducts more current for a given size. Change V3 to 1.25V and the multiplier on M1 to 100 to check this assertion.

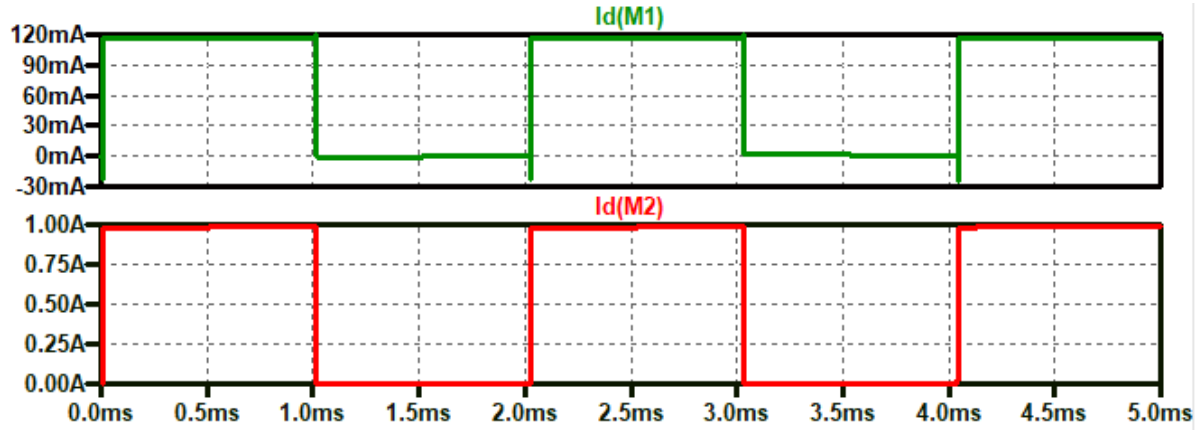


*Figure 16 – PMOS switch conducts more current*

## Final Design of the 1.25V Supply with Real Components

We now pull everything together to design the final circuit. The poles of the output filter have been moved to a higher frequency when we reduced the size of the inductor. We also want a larger capacitor to smooth output transients. With a 2µH inductor and a 100µF capacitor our poles are at 11kHz. Because $f_0$ has increased we should also move our zero upward. Recall from the AC analysis of the error amplifier that the higher we move the zero the move gain we will have at low frequencies (we want high gain to quickly bring the supply's output to the desired voltage).

Before we do that let's also increase the size of R2 to avoid loading the output of the opamp. We maintain the same ratio: R2 will now be 10k and R1 is 400k. If we move the zero up to about 10kHz we have:

$$C_1 = \frac{1}{2\pi * 10k * 10k} = 1.59nF$$

$C_2$ is then set at 159pF. This is implemented in both an ideal and real version. See **Supply_125V_3_Ideal.asc** and **Supply_125V_3_Real.asc**. One issue is overshoot up to 1.6V with a 3V supply and about 1.74V with a 5V supply (both with resistive load). One corrective is to reduce the conductivity of the main switch. This simulation had a PMOS switch with size of 600nm/120µm and M=20. Results are shown in Figure 17. The current through R6 is the load current, which starts at nominally 100mA before decreasing to 40mA and then 5mA.

We will make a few additional changes to this design as we continue but Figure 18 shows the overall schematic of this circuit for reference. The topology will remain very similar.

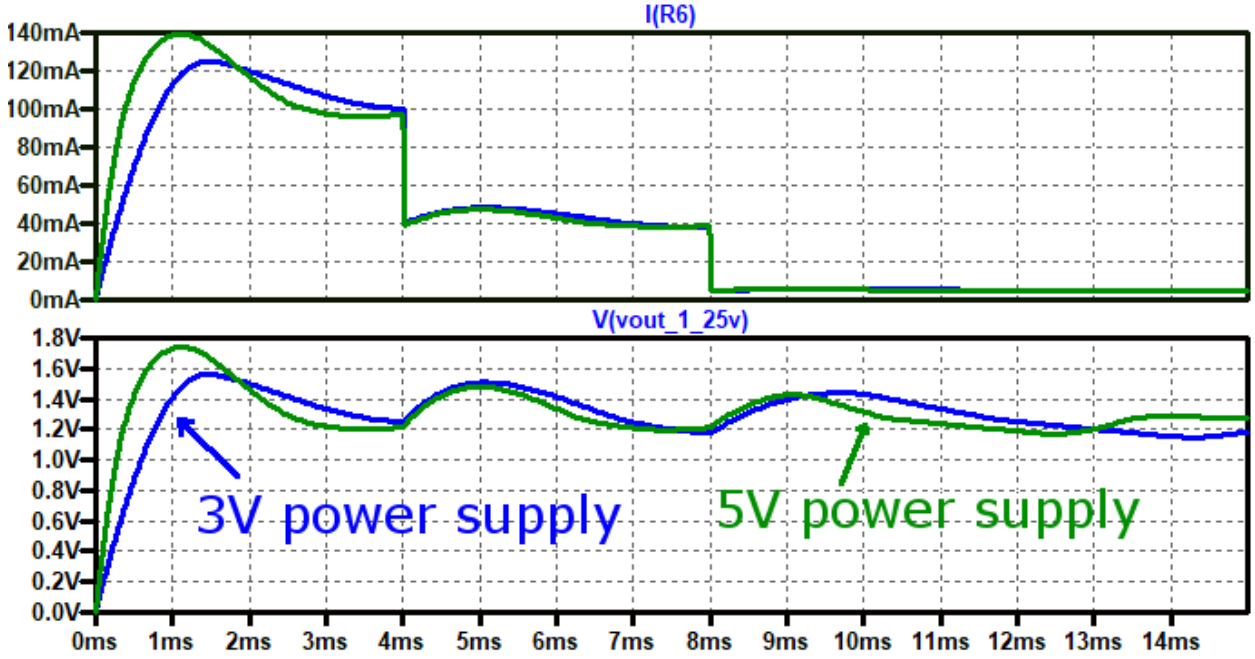


*Figure 17 – Transient response of the 1.25V supply*

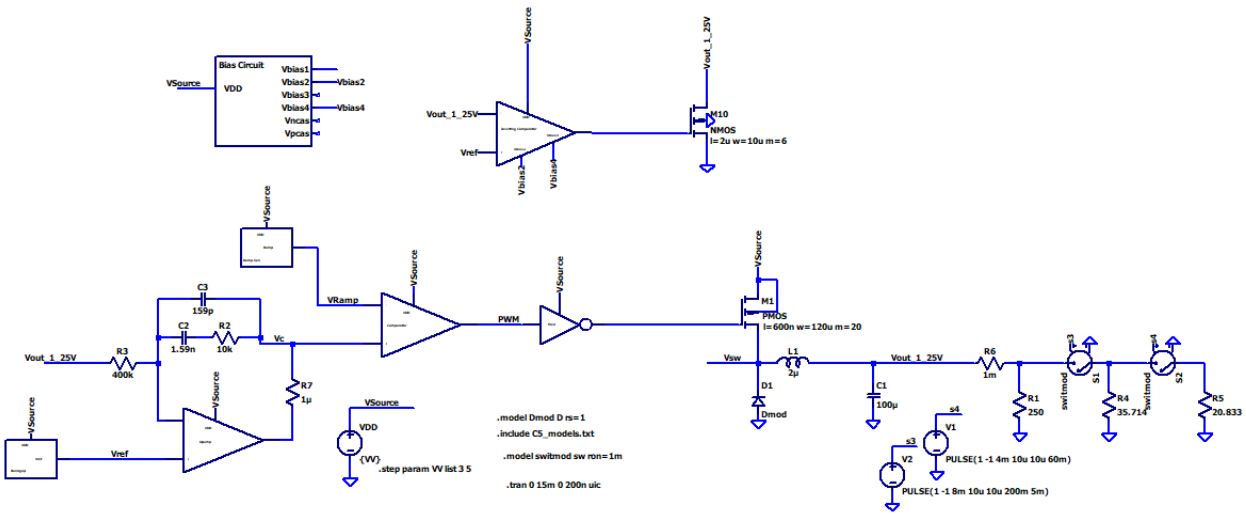


*Figure 18 – 1.25V supply complete top-level schematic*

# Design of the 2V Power Supply

The two volt power supply has design challenges not found in the 1.25V supply. The bandgap reference of 1.25V cannot be directly compared with the output voltage by the error amplifier for this supply. We will instead use a resistive voltage divider so that when the output of the supply is at 2V the voltage divider produces 1.25V for the error amplifier. An advantage of this arrangement is that we have a fixed DC load on the output that can help provide stability. We may not need to provide the active minimum load we used for the 1.25V output supply. We copy the main design parameters from the 1.25V supply. The parallel combination of the voltage divider should have a resistance of 400kΩ. The ratio $R_1/(R_1+R_2)$ should be 1.25/2 = 0.625. (If the output is at 2V the control circuit input will be at 1.25V.) Solving the second equation:

$$R_1 = (R_1 + R_2) * 0.625$$

$$0.375R_1 = 0.625R_2$$

$$R_1 = 1.667R_2$$

If $R_1 * R_2/(R_1+R_2)$ = 400kΩ then substituting the above result we get $R_1^2*0.6/R_1*1.6$ = 400kΩ. Therefore $R_1$=1,067 kΩ and $R_2$=640 kΩ. Note that this configuration will only draw about a microamp from the output so we may need to reduce the size of these resistors.

While simulating the power supply designs with the real transistor models there is a very noticeable sluggishness to the simulations. One optimization that can be done is to break the bias generation circuit out of the comparator and opamp circuits and produce the biasing voltages externally. This removes the duplication of this circuit and reduces the number of transistors that need simulation. Doing this improvement on **Supply_2V_1_Real.asc** and simulating for 1ms reduced the computer time needed from 36 seconds to 23 seconds, a 36% reduction!

In Figure 19 we see the simulation results from **Supply_2V_2_Real.asc**. Peak overshoot is about 2.41V,

which seems reasonable for our simple control loop. The schematic in Figure 20 shows the aforementioned voltage divider on the input of the error amplifier as well as the bias circuit broken out into a separate schematic block.

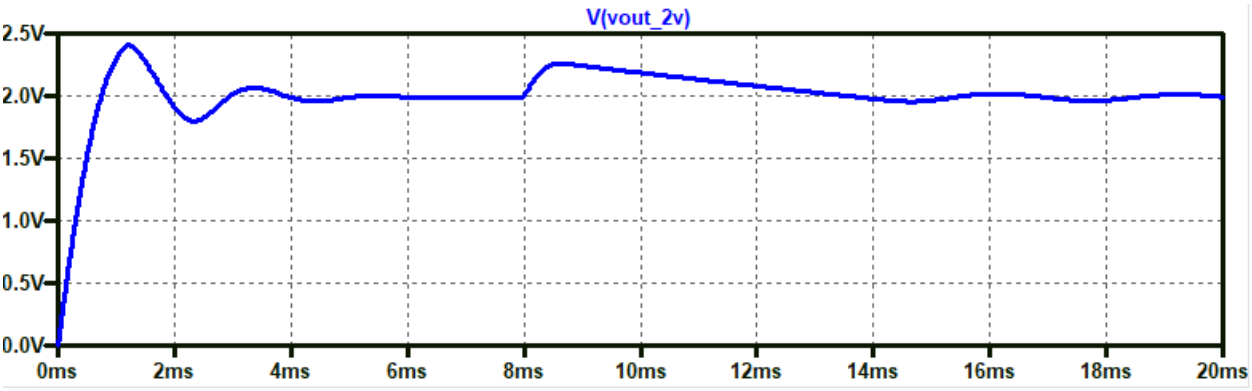


*Figure 19 – Transient response of 2V supply*

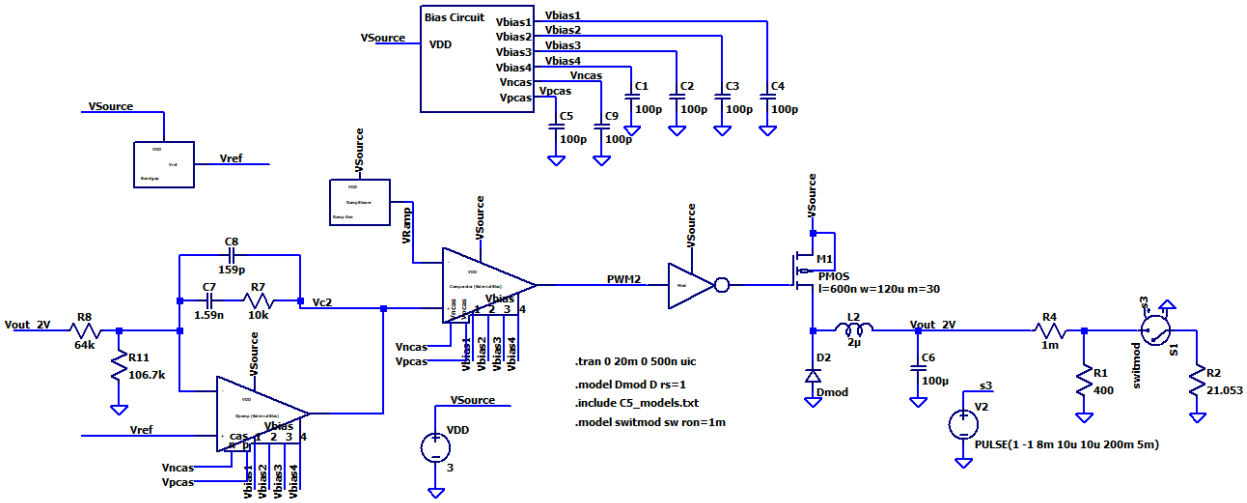


*Figure 20 – 2V supply schematic*

## Design of the Negative Voltage Supply

There are a few special features of the -500mV supply. A negative voltage presents some challenges that will be discusses with regard to well potentials and the possibility of forward biasing some body diodes. Another item of interest is that this rail only needs to supply 100µA, max. Because of the small current required it is feasible to implement this supply with a relatively simple charge pump. A charge pump is in general less efficient than a buck supply, for example, but when extremely small currents are required from the supply the power required for the control circuitry (opamp, comparator) can make the charge pump a more attractive option. An additional benefit is that the charge pump control is quite simple and stable. The basic topology of the negative charge pump is shown in Figure 21. When an oscillating signal is applied to Vin (usually a square wave) the node at A bounces up and down. The diode D2 clamps A to a maximum voltage of about 0.7V (diode voltage drop). If Vin is swinging 3V then A will theoretically go

as low as -2.3V. The diode D1 will conduct until the output voltage is -1.6V, ignoring charge sharing between C1 and C2.

Because the charge pump is fabricated on-die we cannot use actual diodes (The C5 process does not have “real” diodes). Instead we use gate-drain connected PMOS transistors. The node at point **A** goes negative by a significant amount and the substrate-drain diode could start conducting. There are also problems with the PMOS diode. If the body of the PMOS connected to node **A** goes too negative the p-type substrate to n-well diode may become forward biased. However, if we have the substrate potential be slightly negative this problem is ameliorated. In any event, we avoid specific implementation discussion beyond this as every process will have different requirements and design constraints.

The control circuitry controls whether the charge pump is active of not. When active, a NMOS transistor acts like a pass gate to pass the ramp voltage to a pair of inverting amplifiers. The first is a resistive load amplifier with a low switching point. This is selected because the ramp signal does not swing all the way up to VDD so we need a lowered switching point and low current drain. The second stage is a simple inverter that drives the charge pump. A simulation to determine the switching point of the resistive load inverter is found in **ResistiveInverterSim.asc**. The results in Figure 22 show a switching point of about 1.04V with a 3V supply (the switching point increases slightly as VDD increases). This is very appropriate as the ramp voltage ranges from 0 to 2.1V with this VDD. The NMOS transistor has a minimum length for maximum drive current. Note that a 600nm drawn length results in a 500nm gate length due to lateral diffusion. The PMOS is very long (3µm) to reduce contention current and provide the desired switching point.

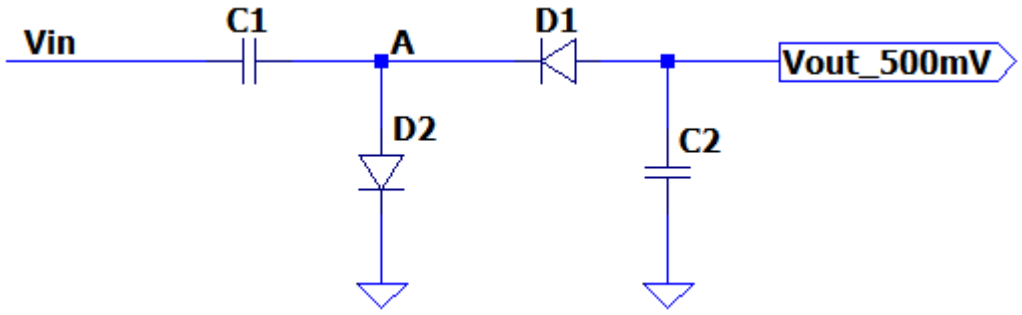


*Figure 21 – Negative Charge Pump Topology*

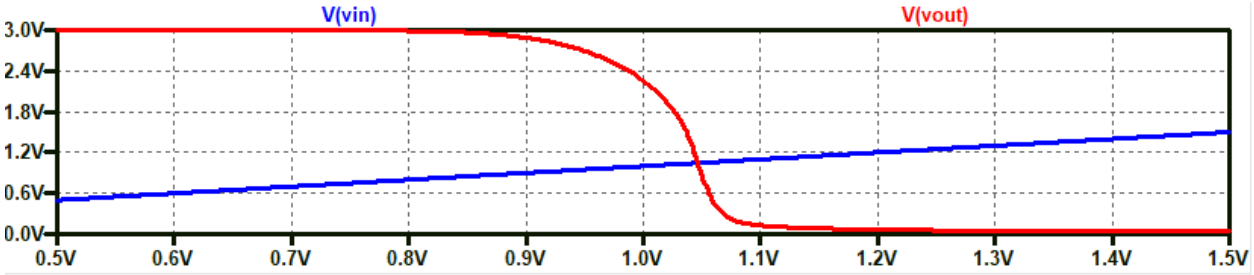


*Figure 22 – Resistive Load Inverter Switching Point*

The primary design concern when designing the charge pump is the size of the capacitors. This is dependent on the load current required and the frequency of the ramp generator. If we assume a load current of 120µA (our control circuit also requires some current) and a frequency of 500kHz (we may

design for a slower PWM) then each cycle may need so supply up to: Q = I*t = 120µA * 2µs = 240pC of charge. When node **A** is at 0.8V (estimated diode-connected voltage drop) on one part of the cycle it drops to -2.2V assuming a worst case scenario of a 3V supply. Accounting for the 0.8V drop across D1 we thus have a difference from the output of -0.5 – (-)1.4 = 0.9V. Given that Q = CV we have for C1:

$$C = \frac{Q}{V} = \frac{240pC}{900mV} = 267pC$$

In our design we have added margin for a larger voltage drop across the MOSFETs and the ability to rapidly reach the desired output voltage during startup by using a 500pF capacitor for C1. For C2 we have selected a value of 100nF, which means that during a 2µs cycle with 240pC of charge removed the output voltage can change by V = Q/C = 240pC/100nF = 2.4mV of ripple, which should be acceptable (<1% of output voltage).

The complete -500mV supply is simulated with a resistive load and real components in **Supply_500mV_FinalSim.asc**. The results are shown in Figure 23. Note that after 0.5ms the load current decreases from 100µA to 20µA, showing the stability of the supply.

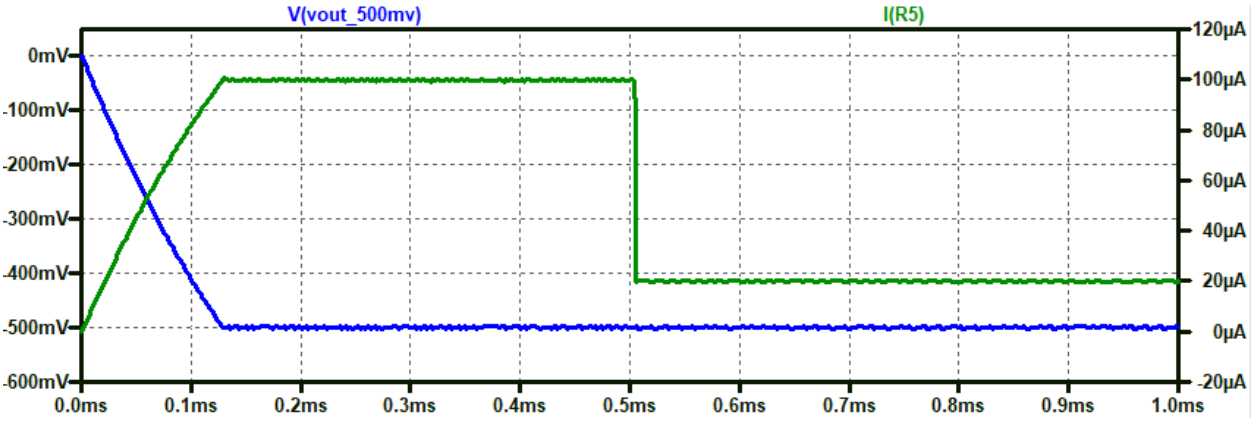


*Figure 23 – 500mV Supply Transient Simulation*

## Testing the Design

The final design needs to be tested over a wide range of operating conditions. We will test under no-load conditions, cross-load conditions, various temperatures, and the full range of operating input voltages. An interesting side note: All these simulations are done on a top-level cell (e.g., **PowerConverter_Real1.asc**) and initially the simulations were not giving correct results. The reason was that apparently the ".include" statement must be in the top level schematic.

One issue that arises is voltage overshoot when there is no load on the power converter. This can be seen in **Simulation_NoLoad_1.asc** and in Figure 24 where the 2V output rises to about 2.7V.

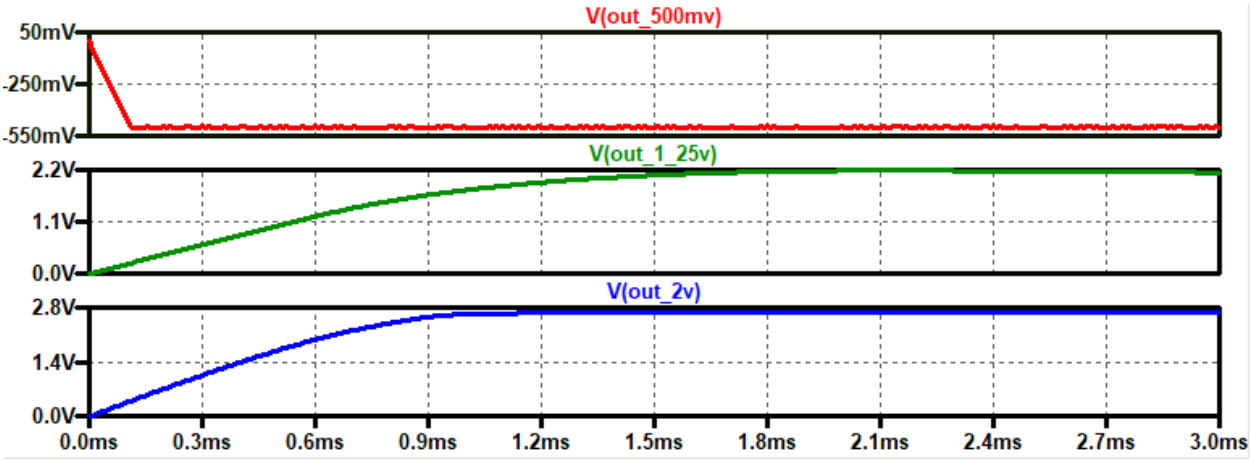


*Figure 24 – No load conditions with excessive output voltage*

We can improve this with a similar system to the active minimum load for the 1.25V system. This time we pull the input to the PWM comparator lower when output voltage rises too high. Using a 105k and 76k voltage divider we need a voltage of 2.172V on the output to raise the negative terminal of this comparator to 1.26V. (Note 1.26/(105/181)=2.172) This is the approximate switching point with the offset discussed earlier. This method of output voltage control almost feels like cheating, although it does come with a cost to power consumption. The results of simulating **Supply_2V_3_Real.asc** are seen in Figure 25. Note that we can see the output voltage flatten whenever the drain comparator rises above the threshold voltage.

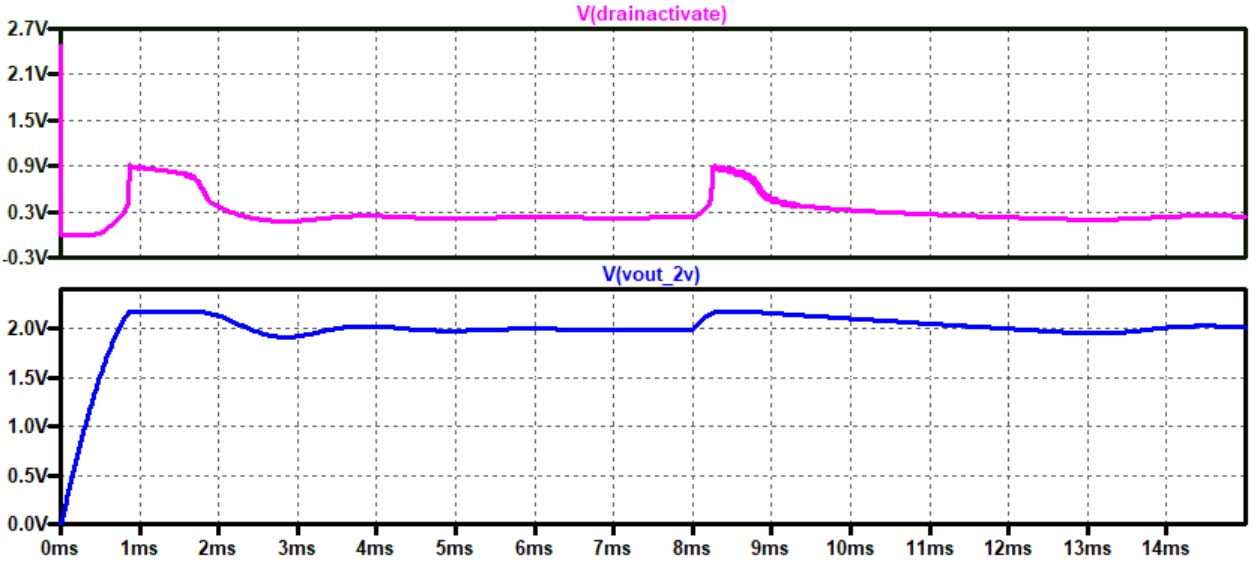


*Figure 25 – Altering the PWM duty cycle to avoid excessive voltage*

## Improving efficiency with a slower ramp

One way that we lose efficiency (energy) is during the switching cycle of the main switches. In **Supply_125V_4_Real.asc** we can simulate the power supply with various voltage conditions and test the effect of using a slower ramp generator. The saved simulation skips the startup transient so we are

looking at a situation where we are mostly steady-state. Table ?? shows significant efficiency gains with the slower ramp. Note you can find the average value of a trace in LTSpice by Control + Clicking on the caption. We clearly see in this case a significant efficiency gain by using the slower ramp (and thus PWM) frequency.

*Table 1 – Efficiency comparison with two different PWM frequencies*

| Ramp Type | Input Power<br>-I(Vdd)*V(VSource) | Output Power<br>V(VOut_1_125V)*I(R6) | Efficiency<br>Vout/Vin |
|---|---|---|---|
| Ramp.asc (~1.4MHz) | 206.12mW | 158.72mW | 77.0% |
| RampSlow.asc (760kHz) | 194.73mW | 179.49mW | 92.2% |

## Another fix to the no-load state of the 1.25V supply

If we look at **Simulation_NoLoad_2.asc** we see that the output of the 1.25V supply easily exceeds 2V. This is a terrible overshoot and unacceptable voltage regulation. We could add a large passive load but an easier method is to repeat what we have done for the 2V supply and reduce the PWM duty cycle when output voltage rises too high. We again put a resistive voltage divider on the input to the comparator as seen in Figure 26 from **PowerConverter_Real3.asc**. (See node Drain_125V) The results seem quite promising. Note that we simulate at both 3V and 5V supply voltage and a range of temperatures from 0 to 75 degrees Celsius.

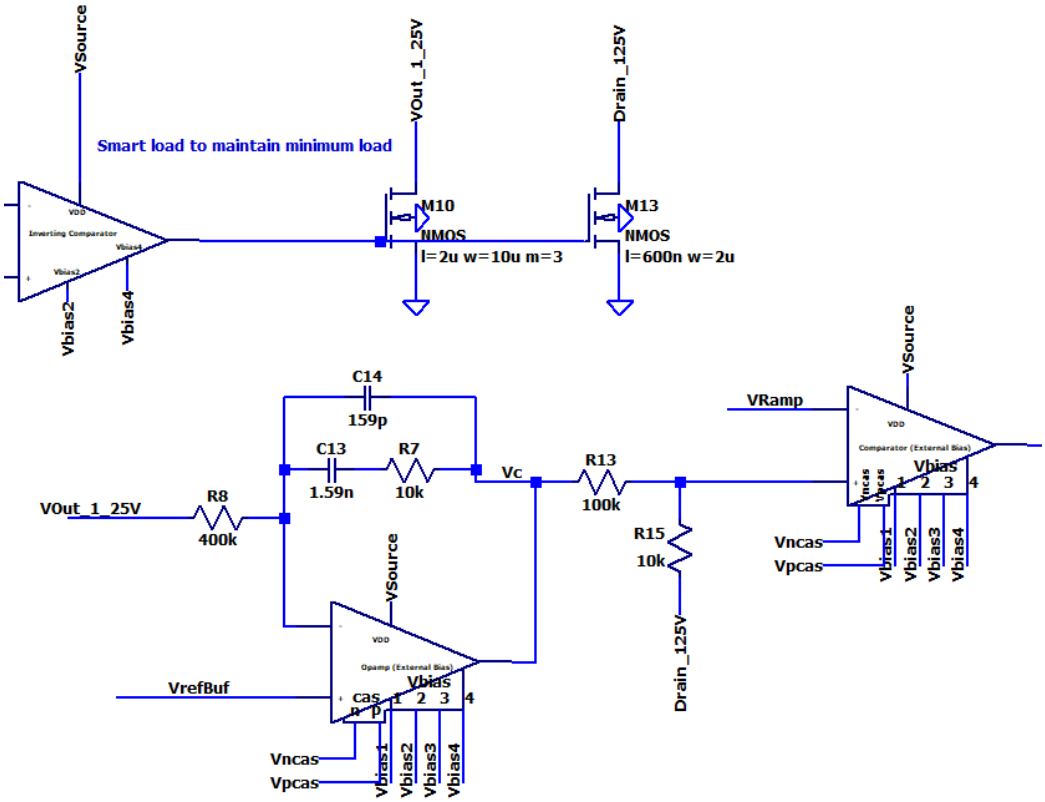


*Figure 26 – Adding over-voltage control to the 1.25V supply*

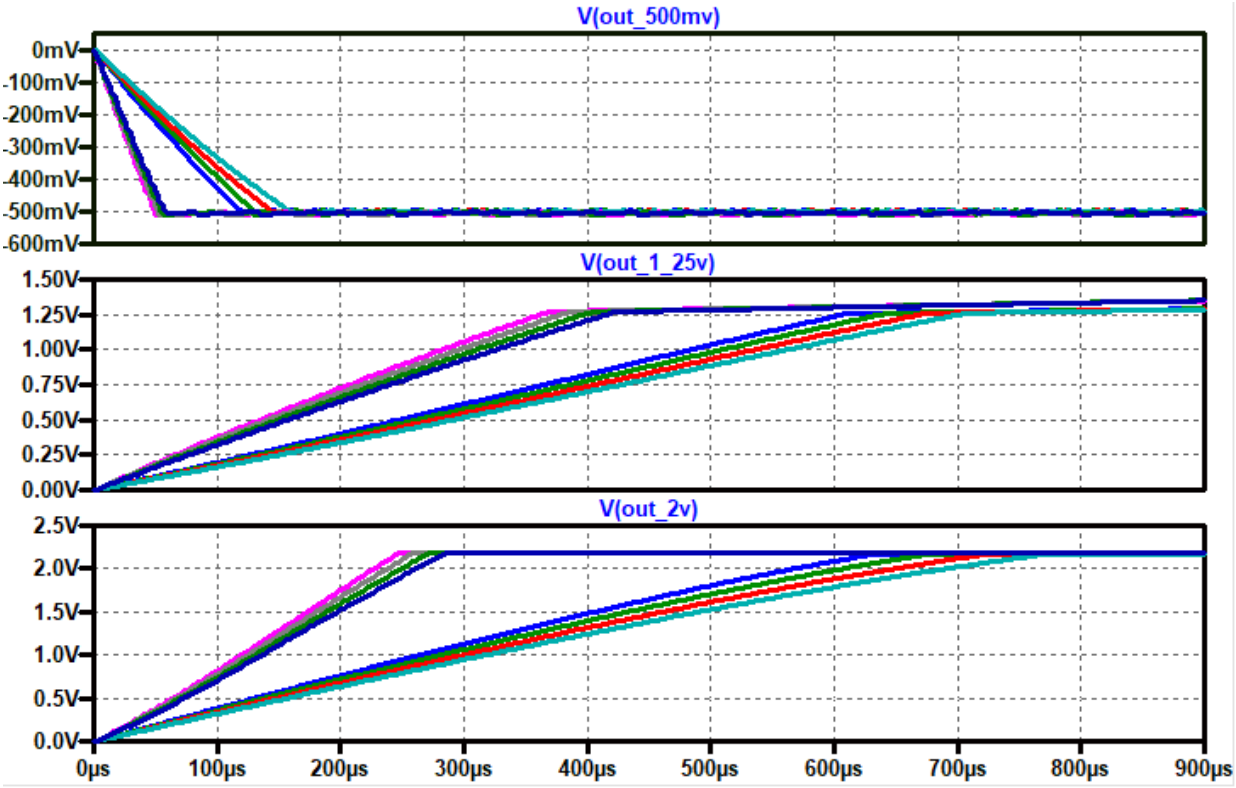


*Figure 27 – No load simulation with a variety of voltage and temperatures*

## Final Simulations

In Figure 28 we have a full load simulation from **Simulation_FullLoad_1.asc** where the three supplies begin at a full load until somewhere between 1.5ms and 2.5ms. Note that we simulate with both a 3V and a 5V supply voltage. Output voltages remain reasonable with perhaps the 2V supply running a little high at approximately 2.2V. Output voltage remains largely stable as the load currents decrease.

It is worth commenting that there is another method of running these simulations. The majority of the simulations in this report use resistive load elements (a.k.a. resistors). We can also use current sources to simulate a different type of load. In Figure 29 we see the full load simulation with current source loads.

Temperature simulation is done at 80% load in **Simulation_TempSim_1.asc** and can be seen in Figure 30. We simulate the circuit at 0° C, 25° C, 50° C, and 75° C.

In Figure 31 we see the simulation of **Simulation_CrossLoad_1.asc**. Before 1.5ms we see that the 2V supply is fully loaded and the 1.25V supply has a 5mA load. At 1.5ms the situation reverses and we see the opposite cross load condition. As usual, the -500mV supply remains supremely stable.

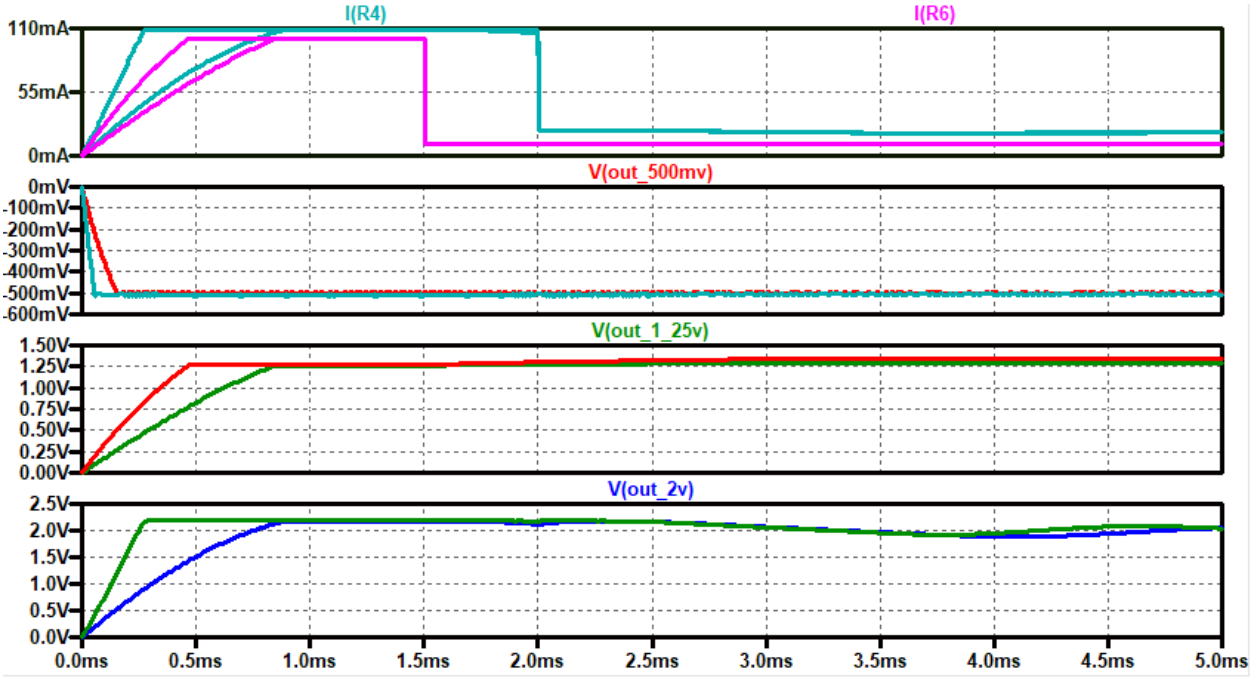


*Figure 28 – Full load simulation*

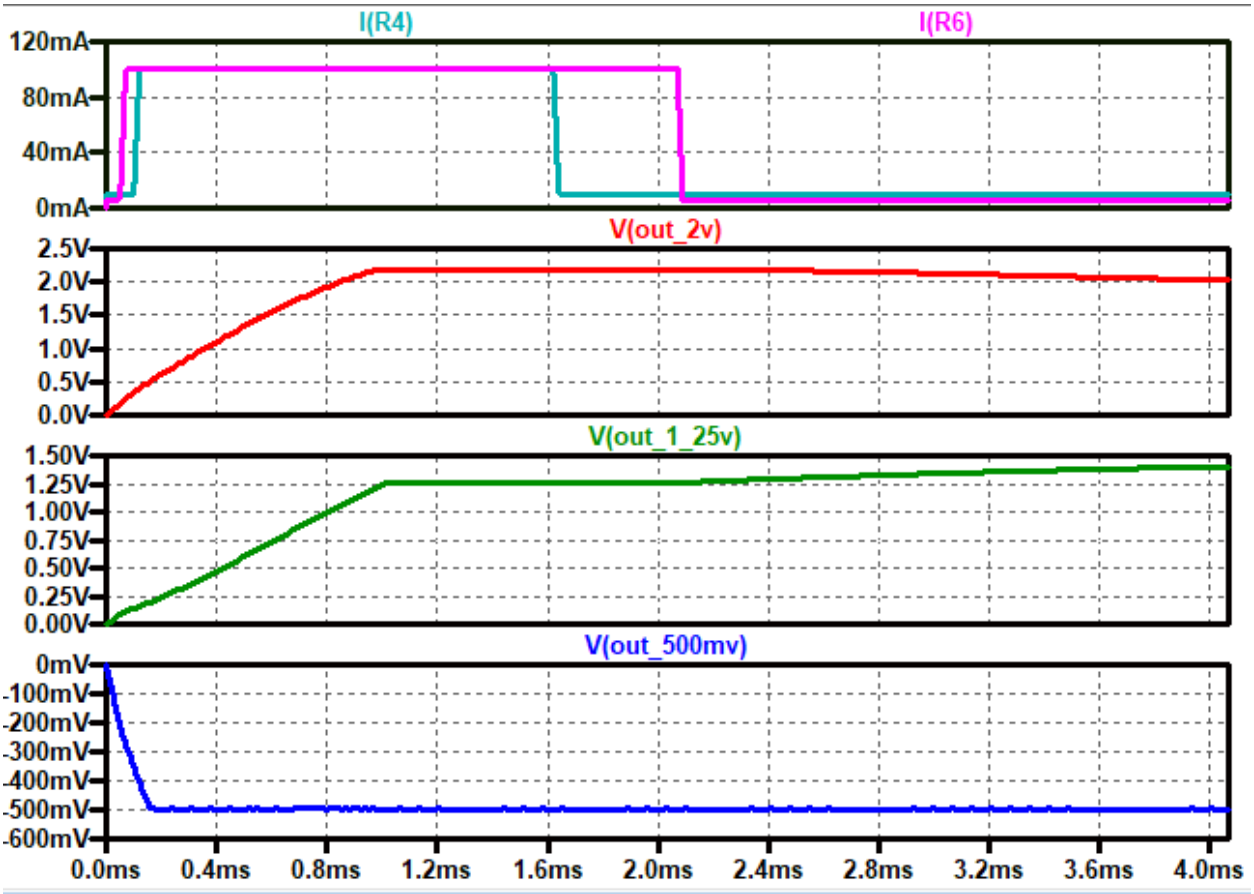


*Figure 29 – Simulation with current source loads*

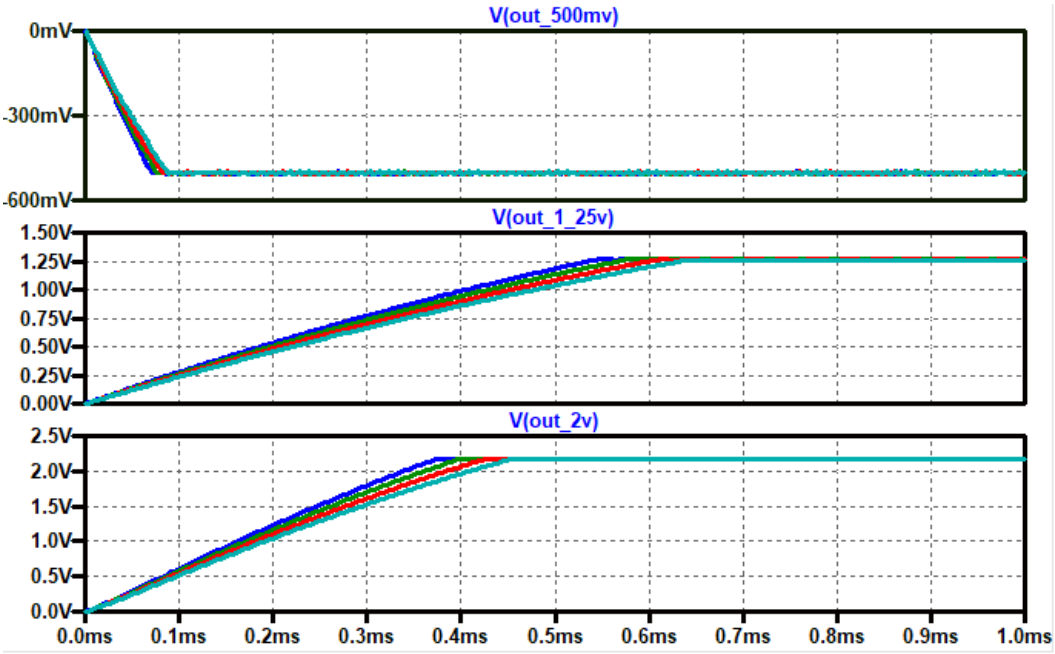


*Figure 30 – Simulation at various temperatures and 80% load*

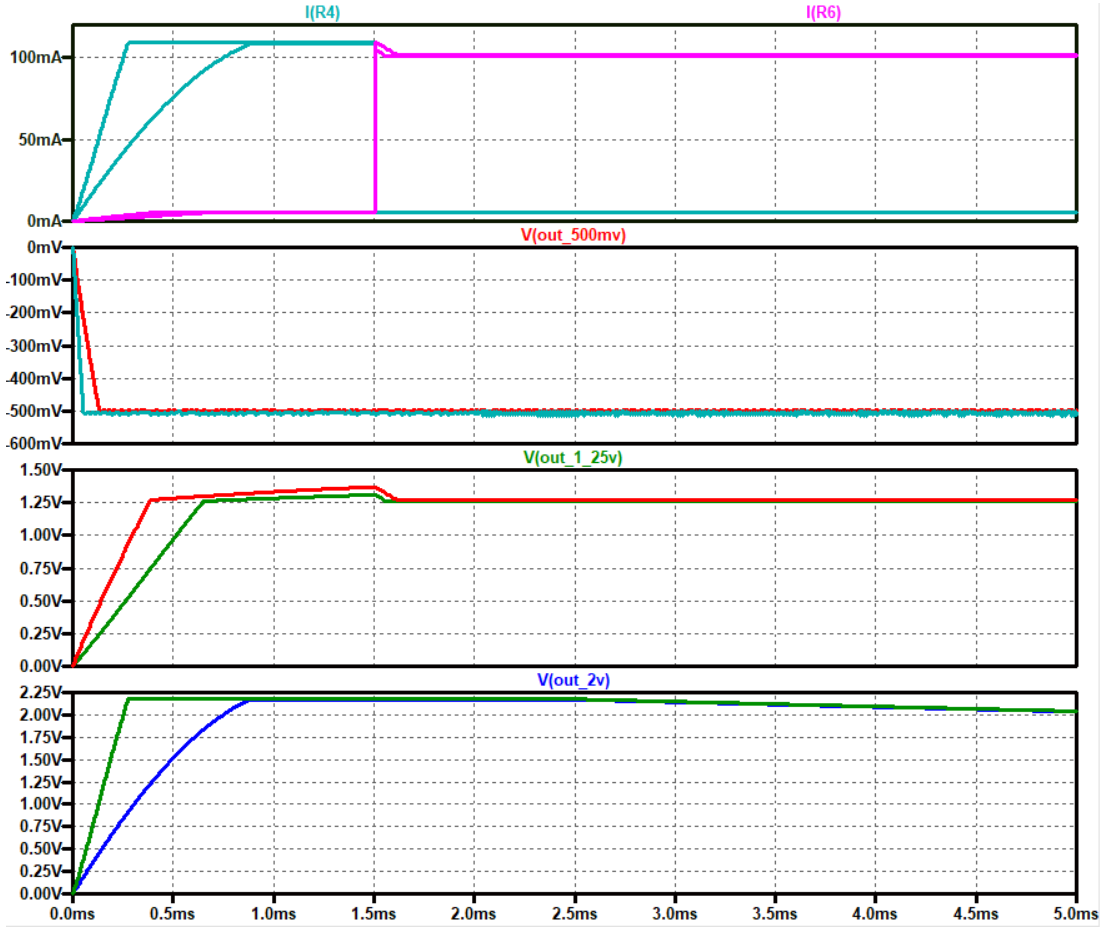


*Figure 31 – Cross load simulation*

## Power Supply efficiency

To test the power supply's efficiency it is important to consider the steady-state environment. During start-up transient events energy is being stored in the output filter's capacitor and inductor, distorting the true amount of power being consumed by the electronics. To speed up our simulation times we use a ".ic" statement to set the initial conditions of the output rails to their steady state values. Note that we simulate for 500µs to try to reach steady state and then average the next 500µs for our power measurements. This may not be totally accurate but should give us an idea of how efficient our supply is at various supply voltages and load currents. The simulation files are **Simulation_Efficiency_3V_100.asc, Simulation_Efficiency_3V_100.asc, Simulation_Efficiency_3V_100.asc, Simulation_Efficiency_3V_100.asc, Simulation_Efficiency_3V_10.asc,** and **Simulation_Efficiency_5V_10.asc.**

*Table 2 – Power supply efficiency*

| Operating Conditions | Input power | Output power | Efficiency |
|---|---|---|---|
| 3V supply, 100% load | 522.81mW | 322.26mW | 61.6% |
| 5V supply, 100% load | 430.85mW | 335.99mW | 78.0% |
| 3V supply, 50% load | 203.22mW | 169.99mW | 83.6% |
| 5V supply, 50% load | 181.79mW | 176.56mW | 97.1% |
| 3V supply, 10% load | 37.03mW | 35.99mW | 97.2% |
| 5V supply, 10% load | 40.37mW | 35.06mW | 86.8% |

One thing to notice is how efficiency increases for smaller loads. This is not generally what we expect for a switching power supply and is due to the main switches being too small. The losses with higher currents result in the low efficiency with large loads. Note that for the 5V supply and 10% load the simulation results here are the average power from 1 to 2 ms as the original time window resulted in an efficiency of 65.7%. This is a good example of how these numbers are a little bit inaccurate.

It would also be instructive to try to examine the individual efficiency of the three voltage rails. For these measurements we will include in the input power the current required to power the "common" circuits such as the bias generator, bandgap, etc. In **Simulation_Efficiency_Isolated500mV.asc** we test at 50% load (50uA) and note that as expected the charge pump design has poor efficiency. Of course, with such a small current supply we don't need good efficiency as the total efficiency is dominated by the larger power supply rails. The load consumes 50.6µW and the control circuitry draws 4.8mW, while the charge pump draws 579.2µW. The efficiency excluding the control circuitry is only 8.7% but drops to about 1% when including that.

In **Simulation_Efficiency_125V.asc** we isolate the 1.25V supply and determine that 127.7mW is consumed by the load. 4.9mW is consumed by the control circuitry, and 248.5mW by the main power switch. The efficiency without counting the control circuit is 51.3%, with it is 50.4%. When we change the main switch to a "more efficient" NMOS transistor in **Simulation_Efficiency_125V_Improved.asc** we get even worse performance at about 43.5% efficiency. We thus give up on pursuing that route.

# Conclusion

The design we have developed uses additional comparators to provide additional load current and/or drastically change the duty cycle for the main switching transistors. This is needed to keep the output voltages within acceptable bounds and avoid (e.g.) a 40% overshoot in the output voltage. In the future it would be interesting to determine if the Type II amplifier and control loop are sufficient to stabilize the output, even when starting from an “off” state under full load and no load.

The decision to use a charge pump for the negative supply made the design process simple although it does result in abysmal efficiency. A step we did take to improve efficiency was separating the common circuitry (bias generator) for all three supplies and avoiding that duplication.

Finally, we tested the power supply under a wide variety of load conditions, temperatures, and supply voltages. The results seem promising and confirm close regulation of the output voltages. Although it seems doubtful that this approach will revolutionize the DRAM industry we have at least satisfied our curiosity.

# References

[1] R. J. Baker, *CMOS Circuit Design, Layout, and Simulation*, Fourth Edition. Wiley-IEEE Press, 2019.